Wireless High-Temperature Monitoring of Power Semiconductors

A Single-Chip Approach

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To my family

Abstract

Because failures in power electronic equipment can cause production stops and unnecessary damage to connected equipment, monitoring schemes that are able to predict such failures provide economic and safety benefits. The primary motivation for this thesis is that such monitoring schemes can increase the reliability of energy production plants. Power semiconductors are crucial components in power electronic equipment, and monitoring their temperatures yields information that can be used to predict emerging failures.

This thesis presents a system concept for wireless, single-chip, high-temperature monitoring of power semiconductors. A wireless single-chip solution is both cost effective and easy to integrate with existing power semiconductor modules. However, the concept presents two major challenges: the implementation of wireless power and communication, and the low-power design of the temperature sensors. To address these challenges, the feasibility of using on-chip coils to provide communication with and to obtain power from an external reader coil is demonstrated, and a low-power, high-temperature bandgap temperature sensor is developed.

For the challenge of generating geometries of on-chip coils with high power transfer efficiencies, a gradient ascent algorithm is used to generate geometries that provide high power transfer efficiency at the frequency of interest. A theory is developed, focused on the relation between optimised coil geometries and the load requirements of an application. A cut-off-point is discovered, beyond which power delivered to the load does not increase even if the load is made lighter. Electromagnetic simulations for an on-chip coil model are presented, which show that this load-limit lies around 10 kΩ for one 350 nm CMOS process. The model is verified with measurements on manufactured devices.

To generate coils which operate within a desired frequency band in which sufficient radiated energy is permitted, a methodology for tuning on-chip coils with on-chip fuses is presented. The decision to use fuses for tuning instead of transistors for this application is due a transistor's requirement of a DC supply for bias. For wireless single-chip systems, no such DC supply is available at system start-up. The methodology presented addresses the challenge of achieving high Q factors for capacitor-fuse series connections despite the fact that the fuse resistance of on-chip fuses is finite in their blown state and non-zero in their active state.

A single-chip, on-chip coil solution comes with advantages such as galvanic isolation from the power device and simplicity of integration in existing modules. However, because a wireless design with a small on-chip coil will limit the amount of available power, it incurs the disadvantage of requiring a low-power design for the temperature sensor. Therefore, a design is presented of a temperature sensor consuming power in the microwatt range in

the high-temperature region where it is useful for detecting incipient faults, particularly solder faults. This is achieved by compensating for leakage currents that arise in hot reverse-biased p-n junctions, which become significant at these temperatures.

At high temperatures, p-n junction leakage currents can approach or even surpass the level of a circuit's quiescent current. Earlier work on leakage current compensation techniques is examined, compared to and combined with a compensation technique designed to compensate for collector-base leakage in the main bipolar pair of a Brokaw bandgap reference. Experiments show that fully analogue sensors operating at up to at least 230 °C are feasible at a power consumption around 14 µW. Such sensors would yield a resolution of 1 °C if an 11-bit analogue-to-digital converter is employed. However, high-temperature and low-power analogue-to-digital conversion remains future work.

Furthermore, a discussion is held to address design of unimplemented system components which are needed in order to implement a complete single-chip temperature measurement system. Points discussed include high-temperature analogue-to-digital conversion, clock generation and wireless communication.

Contents

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Part I

Chapter 1

Thesis Introduction

It is appropriate to begin a doctoral thesis in industrial electronics with a discussion on *Moore's law*. So without further ado, here follows an introduction within the context of Moore's law driving the development of sensors which can be used to monitor power semiconductors in an elegant way:

Electronic devices are becoming increasingly ubiquitous in our daily lives. Since the 1960s, we have continually been learning how to squeeze roughly twice as many transistors into a given chip area as we could 18 months before, as observed by the prominent Gordon Moore [1]. This miniaturisation trend drives down the cost of integrated electronic circuits while improving their performance in terms of speed and power consumption. The cost of a single integrated circuit (IC) silicon chip today can be as low as a fraction of a euro. One effect of this reduction in price is that a growing variety of sensors are being used to monitor increasing numbers of devices and individuals. In the recent years, we have been using sensors to monitor our elderly [2], our cars [3] and even the people driving our cars [4].

One example of a technology that would be challenging to implement without the advancements that have been achieved in the performance and miniaturisation of ICs is radio-frequency identification (RFID). Currently, *RFID tags* are found nearly everywhere. They are embedded in the plastic proximity cards that allow me to enter my university after it has been closed to the public for the night, but a thesis deadline is almost due. They are used to keep track of cattle [5]. RFID sensors are used to monitor the temperature of food [6]. Some people even allow wireless ICs to be implanted into their bodies, primarily for medical purposes [7–10], but some few do so for the convenience of not having to use a plastic card. Without the improvements in the power consumption of ICs that have been achieved in recent years, many of these applications would pose big—if not insurmountable—challenges to designers, as large coils and an enormous amount of energy would be required to communicate with and power these RFID tags.

Because of our urge to monitor an increasing number of objects and phenomena, it would be beneficial if our sensors could operate over a wide range of temperatures, so that we could place them in harsh environments where we often want to perform the

monitoring. For example, we could use sensors in direct contact with power semiconductor devices in critical power electronic equipment in order to monitor their temperatures for the prediction of incipient faults—and this very topic is the focus of this thesis. One challenge is that these devices are commonly operated at high temperatures, and the leakage current in a silicon chip increases exponentially with temperature, thus making it difficult to design ICs that are able to operate in a power-efficient manner at these temperatures. Of course, of crucial importance is also the efficiency of the wireless power transfer system, which must be able deliver sufficient power to such a sensor. The focus of this thesis is on these considerations. More specifically: How can the temperature range of low-power sensors be extended while still allowing them to remain just that, *low-power* sensors, and how can they be supplied with power?

1.1 Motivation, Problem Formulation and Scope

The reliability of power electronic equipment is of crucial importance in power plants. A sudden failure of a power electronic component in a power plant can lead to power cuts and/or damage to connected components. It is therefore desirable to be able to predict as many incipient faults in power electronic equipment as possible so that preventive maintenance can be scheduled. This thesis investigates how to construct a sensor system that can accurately monitor the temperatures of power semiconductors for the prediction of a common type of fault known as *solder fatigue* [11]. Temperature is a parameter of crucial importance for such a monitoring scheme; thus, the question arises of how to build a system that can efficiently monitor the temperature of power semiconductors. Because of the convenience and many advantages a wireless design brings, it would also be interesting to investigate the feasibility of a wireless temperature monitoring system. More specifically, this thesis seeks to answer the following questions:

Q1: *How can a wireless sensor system be designed in order to predict solder fatigue in power semiconductors?*

The purpose of posing this question is to encourage a discussion of a wireless sensor system in its entirety. What are the advantages and disadvantages of a wireless design, and what parameters are important to measure? In the investigation of this question, another question arises:

Q2: *Is it possible to realise such a sensor system with a single-chip sensor?*

Considering the many advantages of single-chip sensors, the purpose of posing this question is to assess the feasibility of not using any components external to an IC temperature sensor chip, and using an on-chip coil for power and communication.

Q3: *How can a low-power IC temperature sensor be designed to operate at high temperatures?*

As temperatures in the high-temperature range prove to be important parameters to measure, this question addresses how to construct an IC that combines low-power and high-temperature operation.

Q4: *What are critical design considerations and limitations for on-chip coils?*

This question serves the purpose of encouraging the advancement of the theory of on-chip coil design. Because the supply of power is essential to any sensor system, it is important to understand how power transfer efficiency is affected both by coil geometry, but also by system parameters, such as for example the loading of the coil. In addition, it would also be beneficial to comply to radio regulations, so that cheap, small, unshielded sensor systems can be manufactured.

This thesis discusses the design of a monitoring system as a whole. Two main challenges are addressed; how to design the sensing element, and how design the wireless power transfer system. It is found that for a high-temperature IC sensor, the necessity of compensating for the effects of the leakage currents that arise in hot reverse-biased p-n junctions poses a major challenge, and that the loading of an on-chip coil in a wireless power transfer system is of major concern for the power transfer efficiency.

Chapter 2

Condition Monitoring of Power Semiconductors

According to a survey conducted in 2007, 21 % of the failures in power electronic equipment are caused by faults in semiconductors, whereas 13 % are caused by solder faults [12]. These findings represent a significant fraction of all types of failures and suggest that if incipient faults of these types can be detected in advance, then the reliability of power electronics could be significantly increased. Such prediction of incipient faults is commonly referred to as condition monitoring. If an efficient monitoring scheme is implemented, then power plants and other actors in the power electronics industry can perform more cost-efficient, predictable and reliable operations by taking advantage of the ability to perform scheduled maintenance before a catastrophic failure occurs. Avoiding such failures not only reduces downtime but also prevents secondary failures in connected equipment.

The faults that occur in power electronics can be classified into two main types: *package faults* and *chip faults* [13]. Package faults are faults caused by the degeneration of interconnects within the module housing of a power electronic component and include the aforementioned subcategory of solder faults, whereas chip faults occur within a power semiconductor chip. Fault detection methodologies and measures to enable the post-fault operation of power devices have been thoroughly studied in the literature, and many effective techniques are known in the field [14–18]. Such methods allows power electronic circuits to continue to operate, although with reduced performance, even after a device fault has occurred.

In contrast to fault detection, the list of effective methods for the condition monitoring of power electronics is not as comprehensive, particularly with regard to methods for detecting chip faults. An effective method for predicting package faults is to monitor the temperature [19] in order to detect an increased thermal resistance due to a broken or degraded interface caused by either bond wire lift-off or solder fatigue [13]. Methods for predicting chip faults often involve the measurement of multiple parameters and then applying computer-intensive signal processing algorithms to detect incipient faults, as

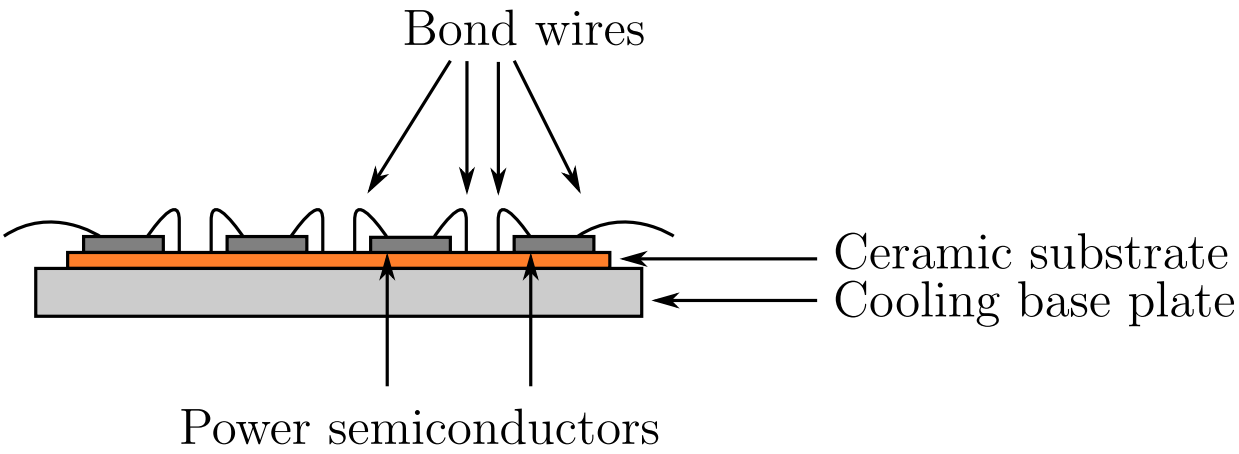


Figure 2.1: Schematic diagram of the cross section of a wire-bond power semiconductor module.

described in [20–24].

One difficulty encountered in condition monitoring for chip faults is that many faults are random and therefore cannot be predicted. An example of such faults is those that are induced by overload conditions caused by external events occurring independently of the chip state, such as lightning strikes [13].

2.1 Device Faults in Power Electronics

As stated above, the faults that occur in power electronic equipment can be classified into two main types; package faults and chip faults.

2.1.1 Package Faults

Figure 2.1 depicts a schematic view of a wire-bond power semiconductor module. Other types of modules exist, such as press pack modules [25], but the scope of this thesis is limited to the wire-bond module. The power semiconductors are soldered onto a ceramic substrate, which is attached to a base plate that provides cooling. Bond wires are bonded from each power semiconductor to the ceramic substrate. The power semiconductors are immersed in a dielectric gel to improve cooling efficiency and to improve reliability in harsh environments by providing protection from dust and moisture.

The primary causes of package faults are *bond wire lift-off* and *solder fatigue* [13]. Both of these occur as a result of differences in the coefficient of thermal expansion (CTE) of one material compared with that of a material to which it is joined. In the case of bond wire lift-off, it is the difference between the CTEs of the bond wire and the silicon chip that causes the fault, whereas in the case of solder fatigue, it is the difference between the CTEs of the ceramic substrate and the silicon chip. During thermal cycling, the different CTEs of the different materials create mechanical stress in the materials. In the case of solder fatigue, voids form in the solder that attaches the chip to the ceramic substrate. The voids that form at the solder interface reduce the cooling efficiency of the base plate,

as the thermal impedance of the interface increases significantly. Hence, the temperature of a power semiconductor will increase in the event of solder fatigue. This increase in temperature may eventually result in the destruction of the device.

In the case of bond wire lift-off, the bond wire eventually lifts and separates from the silicon chip. As in the case of solder fatigue, the thermal impedance changes, although not to such an extent that the cooling efficiency is reduced by a significant amount. However, methods exist for detecting such faults by measuring this change in the thermal impedance [26]. Methods for detecting open-circuit faults (which are a result of bond wire lift-off) in active rectifiers also exist. These methods include *Park's vector method* [27], the *normalised DC current method* [28] and the *slope method* [16, 29].

2.1.2 Chip Faults

The most frequently occurring types of chip faults in power semiconductors are *electrical overstress*, *electrostatic discharge (ESD) damage*, *latch-up and triggering of parasitics*, *charge effects*, *radiation damage* and *thermal activation* [13]. In the following, these types of faults are briefly described:

Electrical Overstress Electrical overstress refers to the case in which voltages or currents exceed their specified maximum values. This can occur as a result of an external event such as a lightning strike, but it can also occur in hot devices, as a high temperature may cause a device to exhibit behaviour that differs from what is expected [13].

ESD damage ESD surges may destroy the gate oxide of a power semiconductor. Partial damage to a device may occur before mounting and go initially unnoticed during operation, eventually causing a gate short. The shorting could occur even several years after mounting.

Latch-up and triggering of parasitics An overly rapid switching waveform can trigger parasitic elements in a semiconductor and drive the device into a latched-up state, which in turn leads to device failure due to excessive current and/or temperature.

Charge effects Charge may accumulate in the gate oxide over time. This is caused by either hot-carrier injection, in which high-energy electrons are injected into the gate oxide, or by ionic contamination, in which ions become trapped inside the power semiconductor during the manufacturing process and then distort the electric field within the semiconductor throughout its lifetime. The former phenomenon is common for devices that operate at high temperatures [13].

Radiation damage Radiation can cause displacements and ionic damage in a power semiconductor. This effect is of major concern for applications where the radiation dose is high, such as in nuclear reactors, particle accelerators and in space.

Thermal activation Many degradation processes in power semiconductors are thermally activated. That is, they are governed by the Arrhenius relation [30], which means that their rates of degradation are exponentially related to the ratio between the temperature and the activation energy.

Some of the faults listed above are difficult to predict because they are caused by events external to the chip, whereas others are difficult to predict in the sense that for their prediction, several chip parameters must be monitored and analysed. Examples of such parameters for an insulated gate bipolar transistor (IGBT) module include *the voltage drop across the p-n junction*, *the on-state channel resistance*, *the injected turn-on gate charge*, *the collector current*, *the gate-emitter on voltage* and *the temperature* [20].

In contrast to the case for package fault monitoring, complete physics-of-failure models are missing for certain types of chip faults. That is, it is not always clear how a certain failure mode affects certain measurable parameters, or a change may be spread out over many parameters and have a magnitude that is very small. Attempts to detect incipient chip faults based on multiple parameters and signal processing have been made, and promising results have been obtained using several algorithms. Examples of such algorithms include principal component analysis [20] and artificial neural networks [21]. These algorithms, however, are not based on an understanding of the underlying physics that causes a device fault, but rather rely on machine learning.

Advanced gate drivers can provide more lenient switching profiles for IGBTs than can simple resistive gate drivers and therefore limit the risk of electrical overstress [31]. Measuring parameters such as the temperature and the gate charge profile can yield information that the gate driver can use to optimise the driving process. As an example, one method of gate driving is to limit the time derivatives of the gate voltage in different regimes of operation [31]. This permits a faster switching process than is feasible with a resistive gate driver while maintaining safe operation. Faster switching, in turn, reduces the amount of heat generated in the switching device, thereby extending its life.

2.2 Temperature Measurements in Power Semiconductor Modules

This chapter is concluded by stating that temperature is a parameter of crucial importance for the condition monitoring of power semiconductors and by providing a summary of a few methods used to measure the temperature in power semiconductor modules.

Temperature can be used to detect solder fatigue and bond wire lift-off. It is also used in many chip fault monitoring schemes and can be used for fault prevention in gate drivers.

The remainder of this section is dedicated to related work on temperature monitoring systems for power semiconductor modules.

2.2.1 Physical Modelling of the Package

A 3-dimensional (3D) model of a power semiconductor module may be created to estimate the temperature of the power semiconductors residing within it [32]. In such a set-up, the temperature at, for example, the base plate is measured and used in combination with the model to estimate the temperatures at other locations within the module.

A disadvantage of this approach is that it may require considerable computational power if, for example, finite-element method (FEM) simulations are used, and it may not always be feasible to model all aspects of the module [32]. Another disadvantage is that it can be costly and time-consuming to develop accurate 3D models of power semiconductor modules.

2.2.2 Temperature Dependence of the Gate Resistance

The temperature of a power semiconductor can be estimated by measuring the gate resistance and considering its temperature dependence. The gate resistance can be estimated by analysing the turn-on waveform of an IGBT or a metal-oxide semiconductor field effect transistor (MOSFET) [33]. A challenge with this approach is that the process of analysing the waveform requires a high sampling rate measurement system.

2.2.3 Temperature Dependence of the Collector-Emitter On-Voltage

Another parameter that is sensitive to temperature is the collector-emitter (CE) on voltage of an IGBT, $V_{\mathrm{CE,\,on}}$. A measurement technique for estimating this voltage has been developed and consists of two parts: off-line characterisation of the IGBT and on-line measurements of $V_{\mathrm{CE,\,on}}$ by a circuit incorporated in the gate driver [34]. This approach shares the challenge of requiring a high sampling rate with the approach of estimating gate resistance.

2.2.4 Integrated Temperature Sensor in the Power Semiconductor Chip

It is possible to integrate a temperature sensor within the power semiconductor chip [35]. In this way, the temperature can be accurately monitored because sufficient power is available and the distance from power semiconductor to temperature sensor is virtually zero. However, this approach requires a redesign of the power semiconductor chip and is thus very invasive. Furthermore, the process technology used for the manufacture of the power semiconductor must include the possibility to integrate devices comprising the temperature sensor, which may increase the cost of the device substantially.

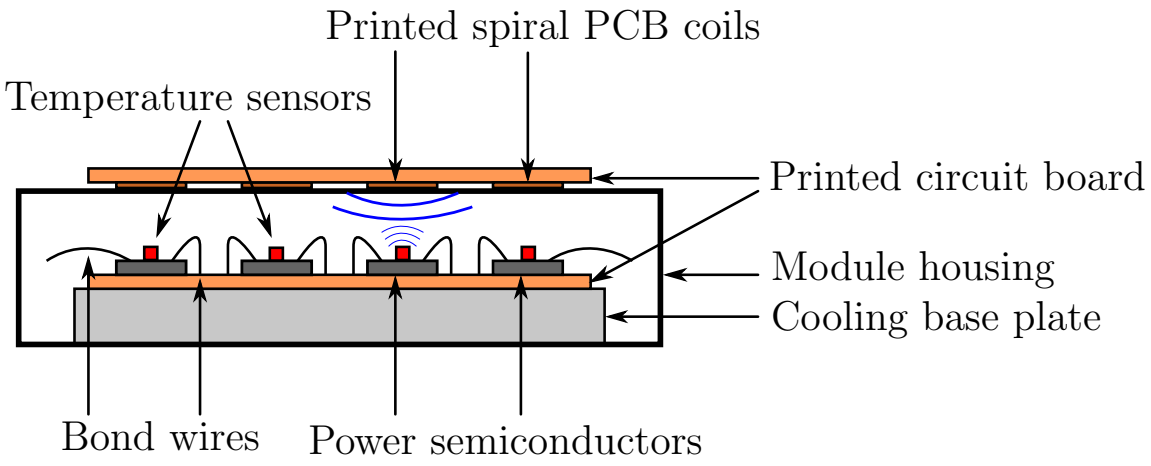


Figure 2.2: Schematic diagram of the cross section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by a nearby RFID reader.

2.3 Single-Chip Wireless Sensors

A schematic view of the basic structure of a wire-bond power semiconductor module is shown in Figure 2.1. The remainder of this chapter presents and discusses a wireless monitoring scheme for monitoring the temperature of power semiconductors soldered to the base plate of such a module. The basic concept, which is also the foundation for the work presented in this thesis, is that a wireless design provides the advantages of galvanic isolation from the high voltages of the power devices as well as ease of integration with existing modules, as no additional components need to be added to the base plate. A schematic diagram of the concept is presented in Figure 2.2. Galvanic isolation from the rest of the sensor system allows the temperature sensors to be glued in direct contact with the power semiconductors to allow accurate temperature readings to be obtained. These readings can then be transmitted via an on-chip coil on the sensor chip. A reader coil mounted externally to, or as part of, the module can receive this signal and can also be used to power the temperature sensors.

This system-level concept for condition monitoring of power semiconductors has not, to the author's knowledge, been addressed in the scientific literature outside of the papers included in this thesis. However, as further elaborated in Chapter 4, on-chip coils have been extensively studied for use in biomedical applications [7, 9, 36]. In the following, advantages of the proposed monitoring concept are presented.

2.3.1 System Integration

In Section 2.2, four approaches to measuring the temperatures of power semiconductors were presented: by using 3D modelling of the package, by measuring the gate resistance, measuring $V_{\mathrm{CE,\,on}}$ and by integrating a temperature sensor in the power semiconductor chip. All of these approaches suffer from the disadvantage that they are difficult to

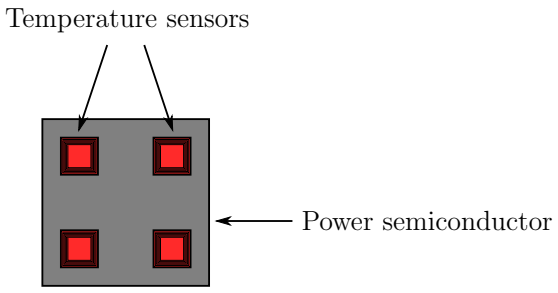


Figure 2.3: Top-view schematic diagram of a power semiconductor. An array of temperature sensors is glued on top of a power semiconductor to measure its temperature distribution.

integrate into existing modules. For the 3D approach, the model can be costly and time-consuming to develop, and infeasible amounts of computational power may be required to obtain accurate measurements [32]. For a gate resistance or $V_{\mathrm{CE,\,on}}$ measurement system, the ceramic substrate must be redesigned to accommodate the components used to take the measurements. A power semiconductor with integrated temperature sensor in the chip is an even more complex and expensive task because it requires a redesign of the semiconductor chip.

The proposed wireless measurement system requires neither complex modelling nor the redesign of the ceramic substrate or power semiconductor chip, at least not as long as the reader coil is mounted outside of the module, because all new components internal to the module are wireless and can be glued on top of existing devices. These devices must, however, be mounted before the module is filled with the dielectric gel.

The possibility exists, however, to place the reader coil and its associated circuits inside the module. If this is done, the ceramic substrate must be redesigned to account for these additional components.

2.3.2 Arranging Sensors in an Array

Traditionally, solder fatigue is detected either by measuring the temperature at a single point on a power semiconductor chip or by estimating it in some way [37]. Although this approach has proven effective, there is room for improvement. If multiple sensors could be glued onto a single power semiconductor, as shown in Figure 2.3, one would have a system that is able not only to measure the absolute temperature at one point at the power device but also to provide information regarding how the temperature is distributed over it. It is possible that such a monitoring scheme would be even more effective for detecting solder fatigue, as the temperature at each location could be compared with those at neighbouring locations. Then, an unusually large gradient would be a sign of the formation of a void in the solder below one of the sensors.

Chapter 3

Low-Power, High-Temperature Sensors

In this chapter, a discussion is held on how a Brokaw bandgap reference can be used as a low-power, high-temperature sensor by compensating for leakage current which otherwise limits the circuit in the high-temperature range. Also discussed are topologies other than bandgap circuits that may be tolerant to leakage currents.

Simulations of a high-temperature Brokaw bandgap sensor are presented in Paper A of this thesis. An IC sensor based on the simulated design was manufactured, and the results of extensive evaluations of this sensor are presented in Paper C.

3.1 Introduction to the Brokaw Bandgap Reference

The Brokaw bandgap reference, originally designed by Paul A. Brokaw [38], is a circuit that is commonly used as a temperature sensor and for the generation of a stable, temperature-invariant voltage reference, also known as a bandgap voltage. One implementation of a Brokaw bandgap reference is depicted in Figure 3.1. It operates by generating two voltages, one that is proportional to absolute temperature (PTAT), V_{PTAT}, and one that has a negative temperature coefficient (NTC), V_{BE1}, which is the voltage over the base-emitter (BE) junction of transistor Q_1. By scaling resistors R_1 and R_2, the first-order temperature coefficients of these voltages can be set equal, and a stable, temperature-invariant voltage, V_{REF}, can be generated by summing V_{PTAT} and V_{BE1}.

3.1.1 Generation of the NTC voltage

The BE junction of a bipolar junction transistor (BJT) is a p-n junction, and its voltage-temperature characteristics are therefore identical to those of a silicon diode. Thus, V_{BE1} will have the same first-order temperature coefficient as a diode, that is, approximately $-2\,\mathrm{mV/^{\circ}C}$ [39].

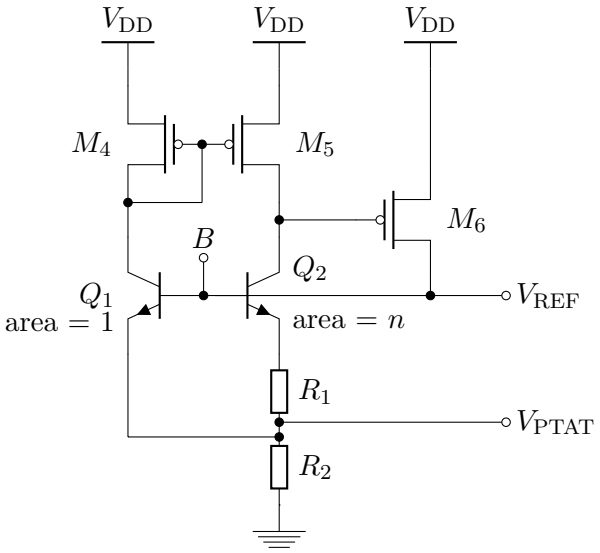


Figure 3.1: Brokaw bandgap reference circuit suitable for implementation in a CMOS process technology. For simplicity, the start-up circuit has been omitted.

3.1.2 Generation of the PTAT voltage

Refer to Figure 3.1. Transistors M_4, M_5 and M_6 constitute a transimpedance amplifier. The current mirror, M_4-M_5, amplifies the difference in the currents passing through either half-circuit and feeds it to the common source transistor, M_6, which amplifies it further. Assuming that M_4 and M_5 are matched, this arrangement will force equal collector currents through Q_1 and Q_2 via negative feedback.

Because Q_2 has a larger BE junction than has Q_1, the current density of Q_2 will be lower than that of Q_1, and hence, its BE voltage drop will also be lower. The voltage across R_1, ΔV_{BE}, will then be equal to the difference between the two BE voltages of Q_1 and Q_2:

$$\Delta V_{\mathrm{BE}} = V_{\mathrm{BE2}} - V_{\mathrm{BE1}}. \tag{3.1}$$

The positive difference between two BE voltages biased at different current densities will have a positive temperature coefficient [38], and thus, the voltage over R_1, ΔV_{BE}, will be PTAT. As the transimpedance amplifier, M_4-M_5-M_6, ensures that the currents passing through the two half-circuits are equal, the current passing through R_2 will be twice as large as that passing through R_1, and hence, the voltage over R_2, V_{PTAT}, will also be PTAT.

3.1.3 Generation of the Stable Reference Voltage

By adjusting the ratio between R_1 and R_2, V_{PTAT}, and hence its temperature coefficient, can be scaled. To achieve a stable reference voltage, V_{REF}, this temperature coefficient should be set equal to that of V_{BE1}, as V_{REF} is equal to the sum of V_{PTAT} and V_{BE1}:

$$V_{\mathrm{REF}} = V_{\mathrm{PTAT}} + V_{\mathrm{BE1}}. \tag{3.2}$$

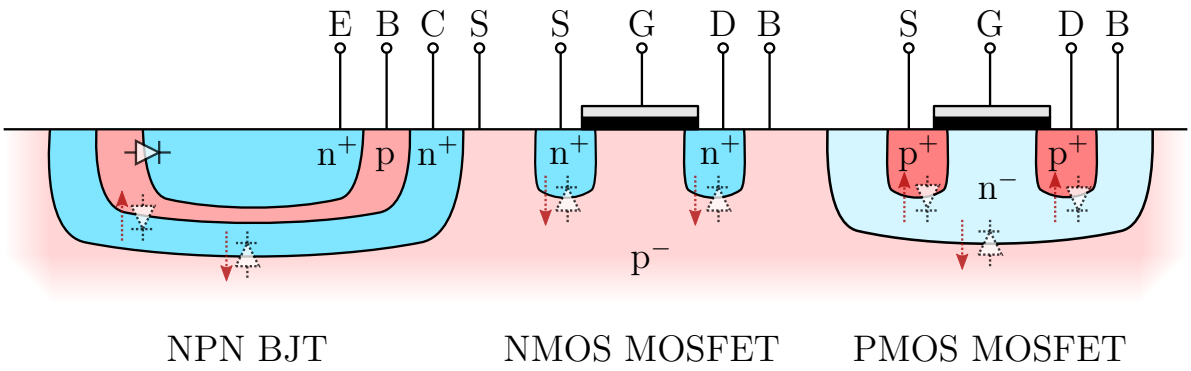


Figure 3.2: Schematic view of leakage currents arising in reverse-biased p-n junctions in an IC. Leaking junctions are illustrated with a dashed diode symbol and an arrow indicating the direction of leakage. The forward-biased BE junction does not generate leakage current when the transistor is in active mode and is illustrated with a solid diode. The emitter (E), base (B), collector (C), substrate (S), source (S), gate (G), drain (D) and body (B) terminal connections of the transistors, as well as doping concentrations, are also shown.

A procedure for the selection of R_1 and R_2 is provided in the appendix of [38].

3.2 Leakage Currents in the Brokaw Bandgap Reference

Leakage currents arise in hot reverse-biased p-n junctions. Leaking junctions for an NPN BJT as well as NMOS and PMOS MOSFETs are shown schematically in Figure 3.2. Reverse-biased junctions are illustrated with a dashed diode symbol and an arrow indicating the direction of leakage. The forward-biased BE junction—which does not generate leakage current when the transistor is in active mode—is illustrated with a solid diode. At room temperature, the magnitudes of these leakage currents are usually negligible, but leakage current is an exponential function of temperature and approximately doubles with every 10 °C temperature increase [40]. Hence, leakage current can be a serious concern at higher temperatures. In the Brokaw bandgap reference, several leaking p-n junctions affect circuit performance. These include the collector-substrate (CS) and collector-base (CB) junctions in the BJTs as well as the source-body (SB) and body-drain (BD) junctions in the MOSFETs.

3.2.1 Compensating for Collector-Substrate Leakage

The effects of CS leakage in the Brokaw bandgap reference have been studied by Radoiaş et al. [41]. They found that CS leakage creates a mismatch in the bias currents running through each half-circuit, thereby limiting the performance of the circuit in the high-temperature range. To compensate for this effect, they introduced a new transistor, Q_3, in cut-off mode connected in parallel to Q_1, as shown in Figure 3.3. The sole purpose of

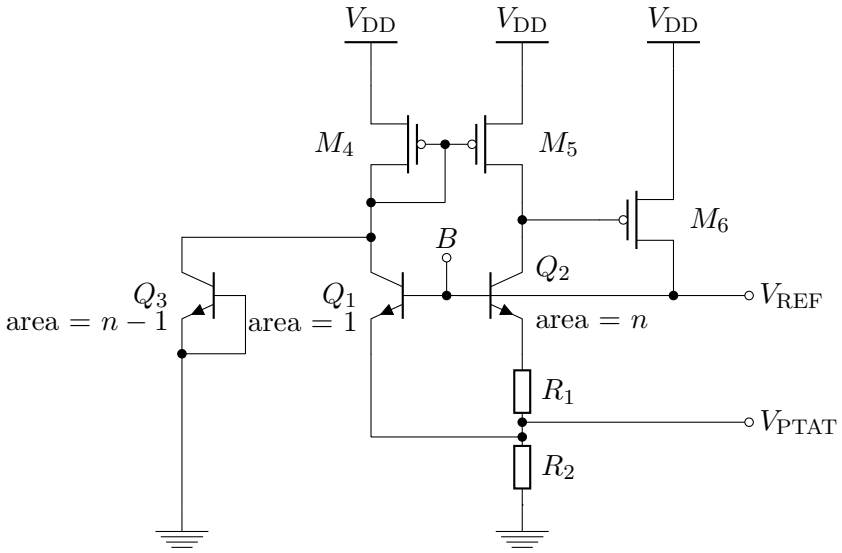


Figure 3.3: Brokaw bandgap reference circuit as implemented in [41]. For simplicity, the start-up circuit has been omitted.

this transistor is to ensure that the CS leakage currents in each half-circuit are matched. With Q_3 in cut-off mode, it does not affect the circuit performance in any other aspect than through leakage current. If the area of Q_3 is equal to the difference in area between Q_1 and Q_2, then the total CS junction area in each half-circuit will be equal, and hence, the CS leakage currents will also be matched.

3.2.2 Compensating for Collector-Base, Source-Body and Body-Drain Leakage

However, Radoiaş et al. did not consider the effects of CB, SB or BD leakage in their work. As argued in Paper A in this thesis, the effects of these types of leakage currents are particularly important for low-power designs, as it is a challenge to achieve a high loop gain around the feedback loop Q_2-Q_1-M_4-M_5-M_6 in such designs.

A low loop gain will not be able to reduce the effect of excess current injected into the bases of the bipolar pair, Q_1-Q_2, to a negligible level. The majority of the current introduced there will follow the lower-impedance path through the BE junction of Q_1 and will thus cause the two half-circuits to be imbalanced. CB leakage from Q_1, Q_2 and Q_3 and BD leakage from M_6 contribute to the injection of excess current and thus must be compensated for. Although not shown in the circuit diagrams of Figures 3.1 and 3.3, an NMOS transistor in the start-up circuit also contributes to SB leakage. Further details about the start-up circuit and SB leakage are presented in Paper C.

Paper A reports simulations of a low-power Brokaw bandgap circuit that compensates for both CB and BD leakage. This is achieved by replicating the sources of leakage through identical transistors in cut-off mode. This leakage current is then mirrored by a circuit presented by Mizuno et al. that achieves good matching of the mirrored current in

reverse-biased p-n junctions by taking into account the amount of reverse-bias applied to the junctions [42].

Paper C presents an evaluation of the circuit presented in Paper A based on experiments performed on an IC chip manufactured using a 180 nm complementary metal-oxide semiconductor (CMOS) process. The conclusion of these experiments is that by using the leakage current compensation techniques described above, the temperature range can be extended by 20 to 50 °C, depending on the desired accuracy. The paper analyses the data at three different levels of accuracy: 3, 5 and 10 °C.

3.3 Lower Limit for Power Consumption

As theorised in Paper A and experimentally verified in Paper C, the power consumption, P, of a Brokaw bandgap reference consists of two components: a linear part, P_{L}, and an exponential part, P_{E}. The power consumption is described by the following set of equations:

$$P(T) = P_{\mathrm{L}}(T) + P_{\mathrm{E}}(T), \tag{3.3}$$

$$P_{\mathrm{L}}(T) = c_{\mathrm{L}}T, \tag{3.4}$$

$$P_{\mathrm{E}}(T) = c_{\mathrm{E}}e^{b_{\mathrm{E}}T}, \tag{3.5}$$

where T is the temperature in kelvin and c_{L}, c_{E} and b_{E} are constants.

For temperature sensors with all the compensation circuits described in this chapter, Figure 3.4 shows the power consumption as function of temperature. From the figure, it can be seen that the temperature sensor has two regions of operation, a linear region where P_{L} dominates, and an exponential region where P_{E} dominates.

3.3.1 Analysis of the Different Components of Power Consumption

In the following, both the linear part, P_{L}, and the exponential part, P_{E}, of the power consumption are analysed.

Linear part of the power consumption The linear part of the power consumption, P_{L}, is determined by the bias current, I_{BIAS}. I_{BIAS} is the current passing though R_2 and is therefore PTAT, because the voltage over R_2, V_{PTAT}, is PTAT. This is the reason as to why it is linearly dependent on temperature. The selected I_{BIAS}, along with the supply voltage determines c_{L}.

Exponential part of the power consumption A regression analysis of the graph of Figure 3.4 in the exponential region yields a b_{E} value of $0.064\,^{\circ}\mathrm{C}^{-1}$. This result suggests that P_{E} is due to the leakage current in reverse-biased p-n junctions, because it is consistent with the fact that the reverse leakage in p-n junctions approximately doubles with every

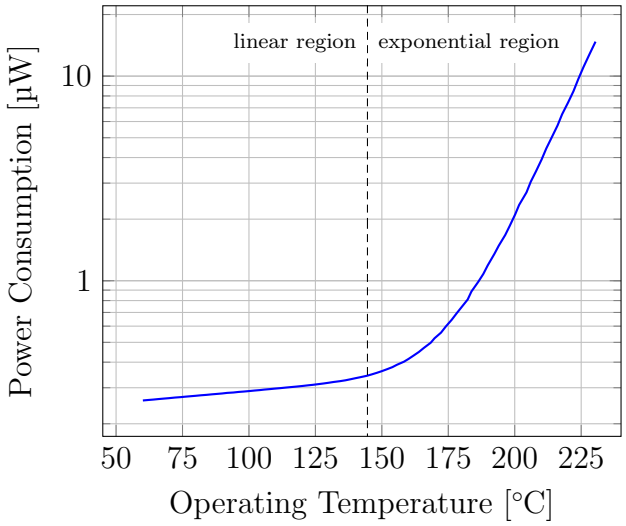


Figure 3.4: Mean power consumption of the temperature sensor described in Papers A and C. The plot has been generated from data from four temperature sweeps presented in Paper C.

10 °C increase in temperature (because $e^{0.064 \cdot 10} \approx 2$). It can thus be concluded that b_E is a constant that will not vary between different silicon-based process technologies or circuits.

The exponential part of the power consumption consists of two components:

- Leakage current: This is the current that arises directly from the reverse-biased p-n junctions in the circuit. All semiconductors in the circuit contribute to this current.
- Replicated leakage current: This is the current that is mirrored from the leakage sources to compensate for CB, SB and BD leakage.

Upon considering the Brokaw bandgap reference without CB, SB or BD leakage compensation circuitry, transistors Q_1, Q_2, Q_3, M_4, M_5 and M_6 will contribute to P_E. Because the leakage current increases with increasing device size, it is beneficial to keep the transistor dimensions small. This also applies when designing the CB/SB/BD leakage compensation circuit, and thus the additional transistors in that circuit will contribute to an increased P_E as well. However, the dimensions of the replica transistors of Q_1, Q_2, Q_3 and M_6 will be identical to Q_1, Q_2, Q_3 and M_6 and therefore, the size of the devices cannot be independently controlled. Furthermore, the leakage current arising from them will be replicated by the current mirror in the compensation circuit. Hence, in the design of a circuit without compensation in mind, transistors Q_1, Q_2, Q_3 and M_6 will contribute three times as much to P_E per junction area as will M_4 and M_5 for which there is no need to compensate for leakage. It should also be noted that one NMOS transistor in the start-up circuit (which was omitted for simplicity in Figures 3.1 and 3.3) contribute to leakage current that should be compensated for and thus also contribute three times to the power consumption per junction area as compared to the non-leakage-compensated transistors, M_4 and M_5.

Because the reverse leakage current per junction area depends on the doping concentrations [43], c_{E} will vary between process technologies.

3.3.2 Selecting the Bias Current

At high temperatures, the power consumption P is dominated by the exponential part of the power consumption, P_{E}. As the exponential part is dominant in this region, reducing the bias current, I_{BIAS}, will have little effect on the total power consumption P. A higher I_{BIAS} is beneficial for the loop gain and will therefore reduce the effects of the CB, SB and BD leakage currents, and thus improve the accuracy of the circuit. For a low-power sensor, it may therefore be wise to select I_{BIAS} to be as high as possible while ensuring that its contribution to the overall power consumption at the highest expected operating temperature, $T_{\max}$, remains acceptable. For example, if $P_{\mathrm{L}}(T_{\max})$ is five times smaller than $P_{\mathrm{E}}(T_{\max})$, one could argue that P_{L} does not significantly affect the total power consumption. Hence, one could strive to satisfy the following condition:

$$5P_L(T_{\max}) < P_E(T_{\max}). \tag{3.6}$$

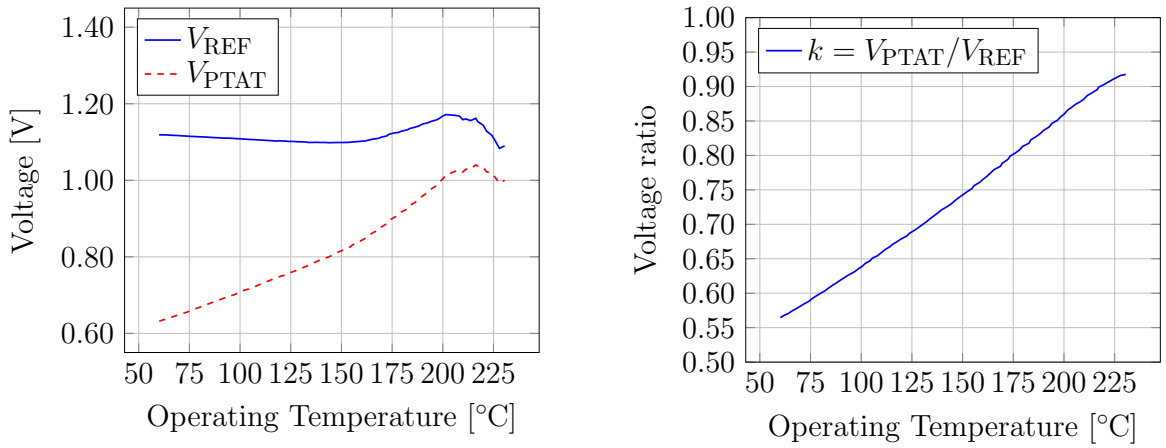
One design methodology for achieving this result is as follows: First, the dimensions of all transistors should be selected while striving to keep P_{E} low, and then, values should be selected for R_1 and R_2 that yield a high I_{BIAS}. The circuit should then be simulated in order to verify that it is functioning correctly. If it is, then the resistances of R_1 and R_2 should be gradually increased until I_{BIAS} is low enough so that the condition expressed in Eq. (3.6) is satisfied. Reducing I_{BIAS} may require readjustment of the transistor dimensions and supply voltage. These factors must also be considered to ensure that the lowest possible power consumption, for a given I_{BIAS}, is achieved.

3.4 Avoiding an Explicit Bandgap Reference

Pathrose et al. have demonstrated that it is possible to build a bandgap circuit without including an explicit bandgap in the traditional sense [44]. In their work, they used two diodes biased at different current densities. Using this topology, they avoid using BJTs. Although not stated in their work, this approach may make the circuit less sensitive to leakage current because leakage sources inherent in BJT designs (CB and CS leakage) are avoided.

They achieved a temperature range of 25 to 225 °C with a power consumption of 90 µW and with an accuracy of 2 °C. This was achieved using an 1 µm silicon on insulator (SOI) process. Comparing these results to the ones obtained in Paper C, which does not use an SOI process, it can be seen that while Pathrose et al. achieve a higher accuracy than the temperature sensor of this thesis, they do this at the expense of a higher power consumption.

Pathrose et al. do not consider the effects of leakage current in their work. If the compensation techniques from Paper C is incorporated in their work, it is possible that the accuracy, temperature range and power consumption can be improved further.



(a) Absolute voltages

(b) Ratio between voltages

Figure 3.5: Measurement results of V_{REF} and V_{PTAT}, as well as the ratio between them, k, as functions of temperature for a temperature-compensated Brokaw bandgap sensor with CS/SB/BD leakage current compensation. The plots have been generated from the temperature sweeps presented in Paper C.

3.5 Accuracy, Digital Calibation and Reference Voltage Stability

In Paper C, it is stated that the accuracy of the temperature sensor can be improved if digital calibration is employed. In this section, estimations are provided for the expected improvements in accuracy a multi-point calibration would yield and the linearity of the sensors are discussed. For simplicity, measurements are shown for a single temperature sensor with an operating temperature up to 230 °C. A temperature sweep based on data from Paper C is presented in Figure 3.5. A plot for V_{REF} and V_{PTAT} is provided, as well as a plot of their ratio, $k = V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$ for a temperature sensor that compensates for CS, SB and BD leakage. Much of the non-linearity present in V_{PTAT} are also present in V_{REF} and can be cancelled by dividing by V_{REF}. Therefore, to achieve the highest possible linearity, k is the quantity that should be sampled. This observation is appreciated when studying the linearities of V_{PTAT} and k in the plots of Figure 3.5. It can be seen that k exhibits a much higher linearity—especially in the high temperature range, where V_{PTAT} even exhibits a negative temperature coefficient. In order to quantify these linearities, below are presented the Pearson product-moment correlation coefficients [45], $\rho_{V_{\mathrm{PTAT}}}$ and ρ_k, for V_{PTAT} and R, respectively, calculated from the plotted data:

$$\rho_{V_{\mathrm{PTAT}}} = 0.988139 \tag{3.7}$$

$$\rho_k = 0.999189 \tag{3.8}$$

For Pearson product-moment correlation coefficients, an absolute value close to unity indicates a strong linearity, while values close to zero indicate a weak one.

From the data of the plot of Figure 3.5b, the sensitivity was calculated. It was seen that R exhibits it's lowest sensitivity between 228 and 230 °C at 600 ppm/°C. Because V_{PTAT} is expected to never exceed V_{REF}, k will never exceed 1. To put the sensitivity value into context, for an analogue-to-digital converter (ADC) to be able to resolve 1 °C, 11 effective number of bits (ENOB) would be required (because $1/2^{11} = 488\,\mathrm{ppm} < 600\,\mathrm{ppm}$). Of course, a higher resolution can be achieved if it is possible to increase the ENOB. However, how large the ENOB can become at the high temperatures involved and with the small amount of power available in our proposed sensor system remains an open question. In any case, it should be noted that for our application, within condition monitoring of power semiconductors, the time scales involved are long, opening for the possibility to achieve a large ENOB by averaging over longer time periods, especially if a $\Sigma\Delta$ ADC is employed [46].

Furtheremore, Figure 3.5a shows that the reference voltage, V_{REF} is stable within 90 mV over the full temperature range between 60 to 230 °C. For comparison, with the same requirement on V_{REF}-stability, the temperature range for a sensor without compensation would be 60 to 164 °C. The range for a temperature sensor compensating only for CS leakage would be 60 to 208 °C. These figures are based on best-case sensors for the temperature sweeps presented in Paper C. For median sensors, the maximum temperatures would be 163, 184 and 216 °C for temperature sensors with no leakage current compensation, with CS compensation and with CS/SB/BD compensation, respectively.

Chapter 4

On-Chip Coil Design

A major driving force behind the study of on-chip coils for wireless power transfer comes from the field of biomedicine, in which it is desirable to be able to implant sensors or control chips into human beings for medical purposes. For such applications, a reader coil is placed in contact with the body at the location of the implanted sensor or controller for communication with the implanted device through its on-chip coil. This situation is similar to our proposed wireless sensor system for temperature monitoring of power semiconductors. One difference would be that an implant communicates through body tissue, whereas a condition monitoring sensor for power electronics would communicate through a dielectric gel. Both of these materials may introduce losses in the inductive link between the reader coil and the on-chip coil, thus reducing its efficiency. For the former case, these losses can be very significant due to the comparatively high conductivity of body tissue, and the tissue's high relative permittivity considering it's primary component is water [47]. A high conductivity enables the formation of eddy currents in the tissue where a significant power absorption occurs. A high relative permittivity increases the inter-turn capacitance of the coils, limiting the trace separation of efficient coils to large values, which in turn limits the number of turns.

In contrast to wireless power transfer through body tissue, the above mentioned challenges do not arise in our proposed monitoring system. Power semiconductors are typically immersed in a dielectric gel of low relative permittivity. Because the gel is a dielectric, very limited eddy currents would arise and because of the low relative permittivity, the trace separation can be kept small, allowing for a larger number of turns than feasible for an implantable device.

4.1 Development of On-Chip Coils

A printed spiral coil (PSC) can be fully characterised by four parameters, denoted W, S, d and N. These are depicted schematically in Figure 4.1 where W is the trace width, S is the trace separation, d is the coil outer diameter and N is the number of turns.

For non-monolithic biomedical implants, an algorithm for the design of PSCs on printed

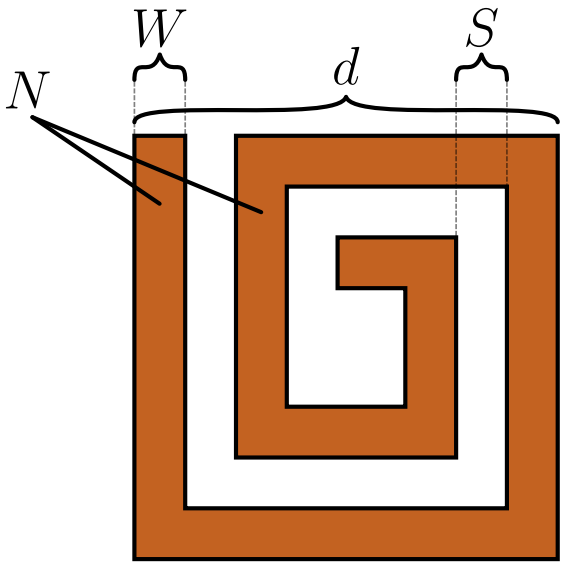


Figure 4.1: Schematic diagram of a printed spiral coil. Shown are the geometry parameters, tracewidth, W; trace separation, S; outer diameter, d; and number of turns, N used to describe its geometry.

circuit boards (PCBs), outputting coil parameters, W, S, d and N, was demonstrated in 2007 by Jow and Ghovanloo [10]. They achieved power transfer efficiencys (PTEs) of 41.2 % (−3.85 dB) and 85.8 % (−0.665 dB) at 1 and 5 MHz, respectively, at a coil separation of 10 mm and with the smaller coil having a diameter of 20 mm. However, their results were based on experiments using coils printed on PCBs only and not IC chips, which are required for the monitoring system of this thesis.

More recently in 2015, Zargham and Gulak demonstrated another algorithm for biomedical implants, this one specifically designed for IC coils coupled inductively to PCB coils [9]. The algorithm optimises the coil geometry using an electromagnetic simulator. Both the IC substrate and the medium between the coils are considered in the simulations. The outputs of the optimiser are the operating frequency and the coil geometry parameters for both the PCB and the IC coils, given the specification of the process technology. Using this algorithm, PTEs of −18.47 dB through 10 mm of air and −20.96 dB through 7.5 mm of bovine muscle and 2.5 mm of air were demonstrated at operating frequencies of 187 and 160 MHz, respectively.

4.2 Load-Dependence for On-Chip Coils

The results in the previous section assume that the on-chip coil is driving an optimum load. For discrete circuits, a matching network with high efficiency could indeed be constructed given the availability of discrete high-Q reactive components, but for ICs, such a task is significantly more challenging. In fact, as is demonstrated in Paper F of this thesis, it becomes more challenging the lighter the load, and thus the lower the power

consumption. The challenge arises because, as the power consumption decreases, the need for larger inductances for the matching network increases, but large inductors are difficult—or even infeasible—to manufacture on-chip and commonly have low Q factors, around merely 10 [7, 9]. Therefore, in Papers D and F, it is assumed that the matching network consists of a single on-chip capacitor which forms a resonant circuit with the on-chip coil. Paper F examines the expected PTE and discusses design considerations which affect it. It is found that there exist a limit for which attempts to decrease the load (that is, attempts to increase the load resistance) do not lower the requirements on the amount of transmitted power required for a constant voltage at the load. For the process technology examined, this limit is found to lie around 10 kΩ.

Since the limit for the load is process technology dependent, it would be interesting to run simulations in order to find this limit for different process technologies. Important technology parameters could then be identified in order to generate a good foundation for selecting process technology. While it is still unknown what process technologies would constitute good candidates for low-power on-chip coil designs, it is likely that SOI technologies would present significant advantages due to their good isolation from the bulk substrate and thus reduced substrate capacitance. Because of this property certain SOI processes are used extensively for radio-frequency (RF) circuits [48].

4.3 Fuse-Based Frequency Tuning

In order to achieve as high PTE as possible at the transmitting frequency, it is important that the resonant circuit, comprising the on-chip coil and a resonance on-chip capacitor, is tuned to this frequency. However, because a single-chip system cannot include a direct current (DC) supply at system start-up and because a tuned capacitor is needed to power-up the system, a transistor-based tuning circuit can not be used because transistor switches require bias. As an alternative to costly laser trimming [49], in Paper E of this thesis, fuses are proposed to be used as the tuning elements. However, a challenge associated with IC fuses is their non-ideal characteristics. A fuse in its blown state will not act as a perfect open circuit, and neither will a fuse in its active state act as a perfect short circuit. Because of these non-idealities, a fuse-trimmed IC capacitor will exhibit a reduced Q factor as compared to a static IC capacitor, so the question arises on how to minimise this Q factor degradation. Paper E presents a method to minimise this degradation by utilising series/parallel combinations of fuses instead of single fuses in an effort to control their resistance contributions in the different fuse states.

4.4 Applications within Biomedical Implants

Although the primary motivation for the work on on-chip coils presented in this thesis is for wireless monitoring systems for power semiconductors, it is worth elaborating on its use within other applications, such as for biomedical implants as mentioned in the introduction of this chapter.

4.4.1 Frequency-Stability of Implanted ICs

One concern for biomedical implants tuned by fuse-trimming could be that due to the dynamics of the host within which an implant resides, electromagnetic properties such as relative permittivity, ε_r, and conductivity, σ, of the materials surrounding the implant could change over time. The concern would be that such a change would result in a change in resonant frequency. Because a fuse-based trimmable capacitor is one-time trimmable, such a capacitor may not be appropriate for implants that require continuous adjustment of the capacitance.

However, because a single-chip implant is small, it is comparable in size to its encapsulation and most of the electromagnetic fields generated by an on-chip coil will be contained within the encapsulation. Because of the weak coupling for PCB-IC inductive links, the external PCB coil and its surrounding media will not have a significant effect on the resonant frequency at the IC side. One concern could be that inter-turn capacitance of the on-chip coil is affected by the permittivity of the surrounding tissues because the fringing capacitance is varying. However, on-chip coils demonstrated in Paper F of this thesis as well as in work by Zargham and Gulak [9] exhibit inter-turn separations on the order of tens of micrometers. If the encapsulation thickness is greater than this separation, the fringing capacitance will be a very small fraction of the total inter-turn capacitance.

In order to verify these claims, electromagnetic simulations of coils, similar to those of Papers D and F of this thesis, were performed. The simulations show that for a 2×2 mm^2 chip coil at a distance of 10 mm to a PCB coil, separated by muscle tissue ($\varepsilon_r = 67.6$; $\sigma = 0.725$ S/m, obtained from [47]) with 1 mm polydimethylsiloxane (PDMS) encapsulation ($\varepsilon_r = 2.9$; $\sigma \approx 0$, obtained from [50]), the capacitor needed for a resonance frequency of 169.4 MHz deviates by a relative value of 16.6 ppm compared to the same simulation set-up, but with muscle tissue replaced with water ($\varepsilon_r = 80.2$; $\sigma = 5.5$ µS/m). The simulations were repeated but with water replaced with vacuum, resulting in a deviation of 4960 ppm.

To appreciate the limitations for the thickness of encapsulation, the simulations were repeated for other thicknesses: 100 µm and 1 µm. The results of the simulations are presented in Table 4.1. The table shows that for a PDMS thickness of 1 mm or 100 µm, the capacitance deviation—and hence the resonant frequency—compared to the case for muscle tissue remain largely unchanged when replacing the muscle tissue with water or vacuum (especially water, which is expected, because it's permittivity is closer to that of muscle tissue than is that of vacuum). However, for an extremely small encapsulation of 1 µm of PDMS, the capacitance can change significantly for the vacuum case, where it will vary with around 17 %, whereas for water it again remained largely unchanged.

Furthermore, because state-of-the-art on-chip coils exhibit low Q factors commonly between 3 and 12 as seen in Paper F as well as in [9] and [7], a change in capacitance of a fraction of a percent will have a very limited and insignificant effect on the amplitude of the generated voltage.

Table 4.1: Simulated values for the relative change in capacitance required to achieve a resonant frequency of 169.4 MHz *for two coils, PCB coil and IC coil, separated by 10 mm when replacing muscle tissue by either water or vacuum as material between the coils. The table lists values for different PDMS encapsulation thicknesses for a 2 × 2 mm² IC coil.*

	Capacitance change [ppm]	
Encapsulation thickness [µm]	*Muscle/Water*	*Muscle/Vacuum*
1000	16.6	4960
100	44.2	5030
1	348	16 800

4.4.2 Ethical Considerations for Implanted Devices

While biomedical implants is a promising technology for the treatment and monitoring of many diseases [51], the privacy of a patient or user should be considered. Because biomedical implants collect personal data from its host, it is important to consider who has the right and ability to access this data, as well as what should be the rights of a patient or user. The author of this thesis is aware of these concerns, and has the hopes that the ethical aspects of biomedical implants are taken into consideration when products and practices are developed, and that laws and regulations prevent malicious actors to take advantage of users in general, but of patients in particular.

Chapter 5

Monitoring System Considerations and Prospects

In this chapter, a discussion is held about the different components of the proposed temperature monitoring system for power semiconductors. What has been achieved is addressed, as well as possible improvements to what has been achieved, what remains to be implemented and various approaches to such implementations. Figure 5.1 shows an overview of a possible implementation of the monitoring system in the form of a block diagram. Blocks with a dashed outline denote subsystems which have not been focused on in this thesis and thus remain future work.

The monitoring system is divided into two parts; subsystems comprising discrete components soldered onto a PCB which is mounted externally on a power semiconductor module, and integrated subsystems manufactured on an IC mounted in direct contact with a power semiconductor. This arrangement is depicted in Figure 2.2, page 12. To provide an overview of the overall monitoring system, in the following, brief summaries are presented of the functions of each of the subsystems.

RF generator and demodulator The RF generator generates the RF signal used by the PCB coil to transfer energy to the IC coil. It should include a demodulator in order to receive sensor information from the IC.

Matching network In order to deliver as much power as possible to the PCB coil, a matching network is employed so that the PCB coil's impedance is matched to that of the RF generator.

PCB coil A current through the PCB coil generates a magnetic field through the IC coil, which in turn generates an electromotive force (emf) voltage at its terminals.

IC coil in resonance circuit The IC coil employs a resonance capacitor in order to boost the emf voltage generated by the PCB coil. The capacitor could also be seen as

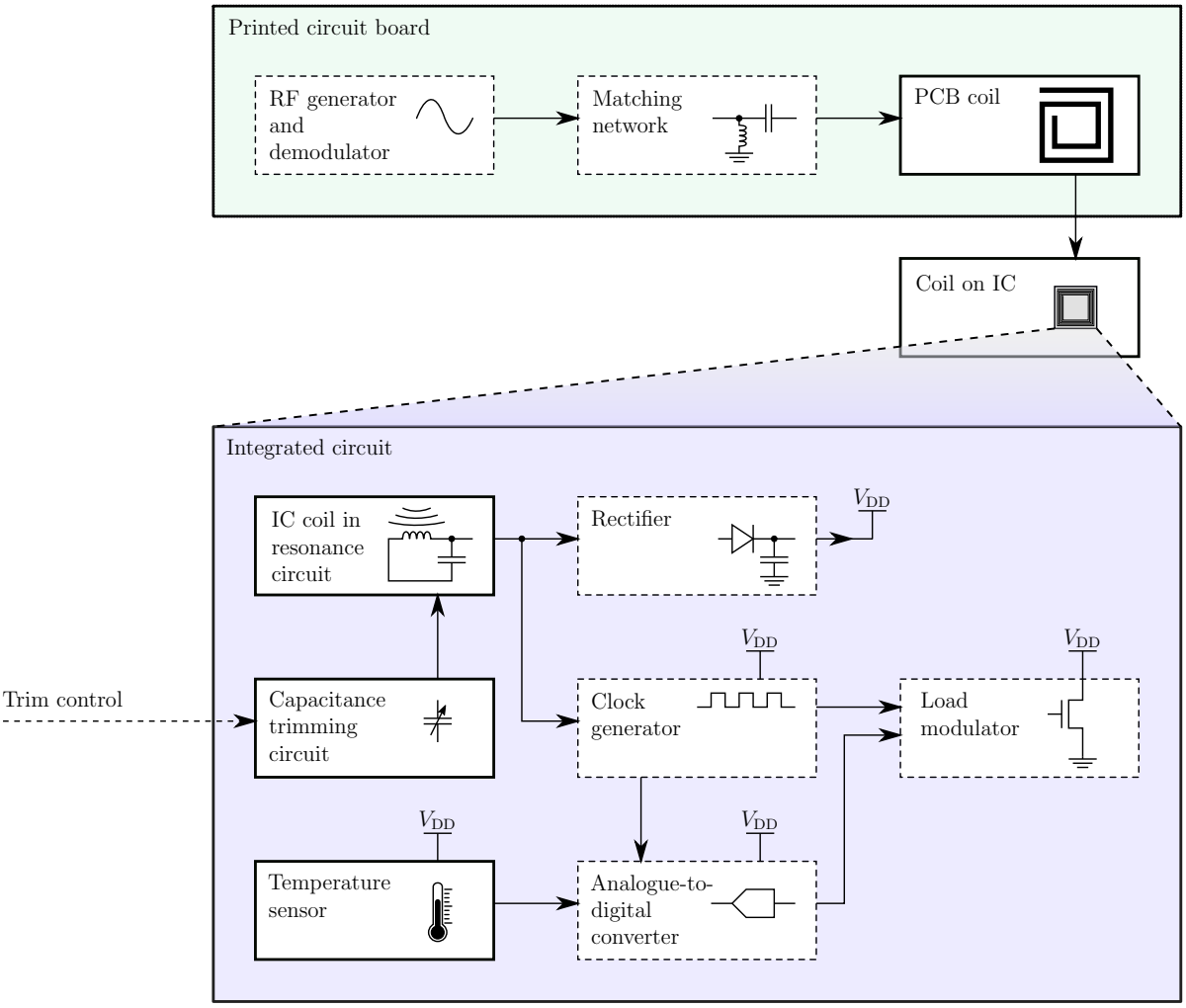


Figure 5.1: Block diagram of the proposed high-temperature monitoring system for power semiconductor modules. Blocks with a dashed outline denote subsystems which are future work, while blocks with solid lines denote blocks which this thesis has focused on.

matching network for the coil.

Capacitance trimmer A capacitance trimming circuit is used to fine-tune the resonance frequency of the resonant circuit so that it lies within the desired frequency band before mounting inside the power semiconductor module.

Rectifier A rectifier is used to harvest the energy from the IC coil in order to generate a supply voltage, V_{DD}. The rectifier should include some form of voltage regulation to avoid delivering a supply voltage that is too high and will harm other subsystems.

Clock generator The frequency content contained within the transmitted power signal can be used to derive a clock signal synchronised with the PCB side. Alternatively, an

internal oscillator can generate the desired clock signal independently.

Temperature sensor An analogue signal representing the temperature is generated by a temperature sensor.

Analogue-to-digital converter An ADC is used to convert the sensed temperature signal to digital form.

Load modulator The digital temperature representation is transmitted back to the demodulator at the PCB side through a load modulator controlled by the clock signal.

In the remainder of this chapter, more detailed discussions are held around the possible implementations of some of the unimplemented subsystems listed above.

5.1 High-Frequency, High-Temperature Rectifiers

In order to avoid complicating the evaluation process of the PTE, a simple, single-transistor rectifier was used for the experiments presented in Paper F. For this reason, the rectifier was designed without consideration of performance at high temperatures at which leakage current may degrade the PTE significantly. For a single-transistor rectifier, there will be a trade-off between on-resistance and p-n junction leakage current. On-resistance decreases with increasing transistor width while leakage current increases with it. Because the high-temperature behaviour was ignored, a very large transistor was used for the experiments of Paper F. In fact, a rough estimation of the p-n junction leakage current consumption of the rectifier exceeds the combined leakage current consumption of all the transistors in the temperature sensor of Paper C of this thesis by a factor of 2.

One method to achieve a high PTE at high temperatures would be to utilise an SOI process, which exhibits very low SB and BD p-n junction leakage current due to isolation of the body terminals from the bulk substrate. However, such processes are more advanced than bulk CMOS and thus may incur an additional cost for the manufacture of the sensor chips. Furthermore, such a technology must be compatible with the other parts of the whole system. For example, the temperature sensor of this thesis utilises high-β NPN BJTs—not a standard device in CMOS processes.

Furthermore, leakage current in MOS rectifiers do not consist only of p-n junction leakage current, but also of subthreshold leakage current for which SOI processes do not offer any advantage over bulk CMOS processes. Due to the lowering of the magnitude of the threshold voltage in MOSFETs with increasing temperature [52], like p-n junction leakage, this type of leakage increases with increasing temperature. Subthreshold leakage could be reduced by the utilisation of ultra-low power (ULP) diodes [53, 54]. However, these devices require control of the body connection even in NMOS devices, which is available in SOI processes, but require a triple-well technology for bulk CMOS.

Another phenomenon that degrades the performance of MOS rectifiers is the voltage drop over the MOS diodes when they are forward-biased. To reduce power consumed due to this voltage drop, threshold voltage cancellation techniques can be employed, where a gate-source bias is added to the MOS diodes in order to reduce their effective threshold voltage, in turn reducing the power consumption due to the forward voltage. These techniques have the tendency to increase subthreshold leakage, but topologies exists which address this challenge. For example, Kotani et al. have presented a high-frequency rectifier where subthreshold leakage is significantly reduced, however again with the drawback of requiring control of the NMOS body terminal [55].

Furthermore, as noted in the introduction of this chapter, the rectifier should employ a voltage regulator in order to avoid damaging the subsystems that it is supplying with power. If the temperature sensor of Papers A and C is employed, one such regulator could be implemented by using the bandgap voltage, V_{REF}, generated by that sensor in order to drive an low-dropout regulator (LDO) that regulates the voltage output from the rectifier.

While it remains future work to examine what the main challenges of high-temperature rectifier design are, it should be noted that several existing techniques already address some of the challenges. However, many of them require more advanced process technologies such as SOI or triple-well technologies and it remains an open question how well they can be adapted for high-temperature operation. Nevertheless, the possibility remains that careful optimisation of simpler rectifiers such as single-transistor MOS rectifiers yield a sufficient PTE for the proposed sensor system and that no new techniques need to be developed.

5.2 Power-Efficient Generation of Clock Signals

The ADC and load modulator subsystems will require a clock signal in order to operate. Thus a clock generator needs to be implemented. However, due to the large temperature span that the IC is intended to operate within, as well as the high maximum temperature, a major challenge would be to keep the temperature drift low. An additional aspect of a monitoring system for power semiconductors is that the temperature could change very rapidly depending on how the power semiconductors are operated. The oscillation frequency of many types of IC oscillator varies strongly with temperature and would change rapidly for a rapid change in temperature. Such a behaviour would put stringent demands on the encoding scheme for the modulator so that the IC clock can be recovered at the PCB side. While temperature compensation techniques for IC oscillators exist [56], a challenge arises in how to extend these into the high-temperature range, up to around 230 °C. Another challenge for high-temperature operation is the increasing power consumption due to leakage current in reverse-biased p-n junctions, as discussed in Paper C, which would limit a low-power oscillation circuit to use only small or few transistors.

One alternative to generating the clock signal fully on-chip would be to derive the clock signal from the frequency content contained in the transmitted signal from the PCB coil. In paper F, the frequency band starting at 169.4 MHz was proposed as transmitting

frequency. However, deriving the clock directly from this signal could result in a too high clock frequency, resulting in a prohibitively high power consumption for a clock divider circuit. Because the dynamic power consumption of a digital circuit is proportional to the switching speed, a very high clock frequency could result in a prohibitively large power consumption. For example, a minimum-size CMOS inverter in a certain 350 nm process consumes approximately 5.5 fJ per transition at 2 V. This would result in a dynamic power consumption of 470 nW per digital transistor operating at 169.4 MHz and could very well be the dominant component of the power consumption for a low-power IC.

5.2.1 Difference between Two Frequencies

This challenge could be overcome if the transmitted signal contains information which can be used to derive a clock frequency significantly lower than the frequencies within the transmission band. The suggested frequency band from Paper F, covers frequencies between 169.4000 and 169.8125 MHz [57] resulting in a bandwidth of 412.5 kHz. If the superposition of two frequencies located at the edges of the frequency band are transmitted to the IC coil, the received signal can then be processed on-chip so that a clock signal is derived, equal in frequency to the difference between the two transmitted frequencies, in our case, equal to the bandwidth of the frequency band in use, which is 412.5 kHz. With a transition energy of 5.5 fJ as in the earlier example, this would result in a power consumption of 2.3 nW per digital transistor, more than a 200-fold improvement compared to the previous case. A clock frequency with such a low power consumption could be suitable for use with digital subsystems within the IC sensor.

This approach would transfer the complexity of generating a clock frequency that is required to be stable in the harsh environment present within a power semiconductor module from the IC to an external PCB where the environment is more lenient and where the available power is significantly greater. An advantage with such a scheme is that a PCB-generated clock would likely be more accurate than an IC-generated clock, presenting better opportunities to other subsystems, for example the ADC, to perform their tasks more accurately.

Which approach to take when designing a clock generator still remains an open question, but it should be noted that numerous challenges that would arise in low-power, high-temperature IC design can be avoided if the required frequency content is derived from the PCB side.

5.3 High-Temperature-Compatible Analogue-to-Digital Conversion and Modulation Circuits

While it likely is feasible to design the full low-power, high-temperature ADC on-chip, such a task comes with a plethora of challenges. Limitations on transistor count and size arise due to the power consumption of leakage current arising at high temperatures while the very same current simultaneously disrupts every node connected to a drain or

a source of a MOSFET and need to be compensated for, further increasing the power consumption and reducing accuracy. Due to the complexity of such a task, the author of this thesis proposes to follow the philosophy presented in the previous section and move as much of the complexity as possible from the IC side over to the PCB side. One approach could be to convert the PTAT voltage provided by the temperature sensor to a frequency which is then transmitted to the PCB side by a load modulator. The frequency could then be recovered at the PCB side by a demodulator and subsequently converted to digital form. This approach greatly simplifies the ADC design by moving a big part of the ADC chain to the PCB side. At the PCB side, power is plentiful and temperatures are not extreme, enabling an accurate conversion process, undisturbed by a high amount of leakage current or by power limitations.

Jeong et al. have demonstrated a low-power, high-temperature IC temperature sensor and ADC operating up to 100 °C at a power consumption of 71 nW [58]. This is achieved by generating a PTAT voltage from a 2-transistor (2T) temperature sensing element [59], and then converting the sensed voltage to a current that drives a temperature-insensitive ring oscillator whose frequency will in turn be PTAT. This frequency is then converted to digital form by the use of counters and an accurate reference clock, also generated on-chip. Because the temperature range of such a sensor does not reach the target, 230 °C, that was set for condition monitoring of power semiconductors, the topology would need to be adapted in order for it to be used in the proposed sensor system of this thesis. One adaptation could be to substitute the 2T sensing element for the high-temperature Brokaw bandgap sensor presented in Paper C. Of course, other parts of the circuit, such as operational amplifiers and the ring oscillator, may need modifications too, in order to address the effects of high-temperature leakage currents, but the implementation details of such circuits are out of scope for this discussion.

The reference clock could either be generated on-chip using the bandgap reference voltage provided by the Brokaw circuit or be derived from the frequency content in the transmitted signal, as described in Section 5.1. As stated in the beginning of this section, another alternative would be to transmit the PTAT frequency from the IC side directly and perform the final conversion to digital form at the PCB side. Because the V_{PTAT} voltage of the temperature sensor of Papers A and C does not increase monotonically in the high-temperature region, to achieve monotonicity for the ADC, the reference clock should be generated by the bandgap reference because the ratio between the PTAT voltage, V_{PTAT}, and the reference voltage, V_{REF}, increases monotonically. The monotonicity of $V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$ can be observed in Figure 3.5, page 22. In this case, both the reference clock and the PTAT clock should be transmitted by the load modulator either by alternating which signal is transmitted, or by some combination of the two signals from which ratio between their frequencies can be derived. For example, the signals could be combined through an XOR gate before transmission.

As with the other parts of the subsystems that remains to be implemented, which approach to take for the implementations of the ADC and modulator/demodulator system remains an open question.

5.4 Concluding Remark

In this chapter, possible implementations and challenges for the unimplemented parts of our proposed sensor system have been addressed. While there is still a lot of work to complete before a complete system can be realised, this overview can serve as a starting point for the design process of several of the subsystems as well as an indication that a complete monitoring system is indeed feasible.

Chapter 6

Conclusion and Future Work

The focus of this thesis is on how to construct a condition monitoring system for power semiconductors in order to predict emerging faults in power semiconductor modules. Specifically, the research has focused on how to extend the temperature range of single-chip, low-power Brokaw bandgap temperature sensors and the design considerations for on-chip coils which are used as receivers for wireless power.

The effects that reverse leakage currents in p-n junctions have on a Brokaw bandgap reference have been analysed. Leakage current compensation techniques, including the work of others, have been developed to mitigate the effects of leakage. Using these techniques, it was possible to extend the temperature range of a Brokaw bandgap reference by at least 50 °C. Although such uncalibrated sensors are not very accurate, digital calibration can be used to significantly improve the accuracy.

A viable approach for designing a wireless system is to use a single-chip solution comprising an IC sensor with an on-chip coil. Such an approach increases reliability and reduces the complexity of the system compared to an off-chip coil approach. Simulations along with measurements on manufactured devices show that it is possible to achieve a power transfer efficiency of $-43\,\mathrm{dB}$ at an average equivalent load resistance of $10\,\mathrm{k}\Omega$.

6.1 Conclusion

This thesis is concluded by providing answers to the research questions presented in Chapter 1.

Q1: *How can a wireless sensor system be designed in order to predict solder fatigue in power semiconductors?*

The idea of wireless single-chip temperature sensors glued in direct contact with the power semiconductors was first presented in Paper A of this thesis. The idea was then further explored in Paper B. A sensor—or an array of sensors—placed on top of a power semiconductor device will be able to detect a change in the temperature (or the temperature gradient in case of a sensor array) which is an indication of solder fatigue.

An advantage with the direct-contact approach is that accurate temperature readings will be provided to the sensor. A wireless design keeps the sensors galvanically isolated from the rest of the system and does not add much to the overall system complexity because the ceramic substrate of the power semiconductor does not need to be redesigned.

Q2: *Is it possible to realise such a sensor system with a single-chip sensor?*

While efficient low-power on-chip coil design has turned out to be a significant challenge, its limitations have been extensively studied in Paper F. The analysis shows that a sufficient power transfer efficiency for the proposed sensor system is possible in order to realise a sensor system operating at an average equivalent load resistance of 10 kΩ. For a complete sensor system, a power consumption of the sensor in the hundreds of microwatts range is foreseen. Simulations along with measurements on manufactured devices show that, for a 10 kΩ load, 100 µW of received power at the on-chip coil would require approximately 5.0 W input to the transmitting coil—a suitable power level for a PCB coil—with a power transfer efficiency of −43 dB.

Q3: *How can a low-power IC temperature sensor be designed to operate at high temperatures?*

In Papers A and C, it was found that in addition to using a previously known CS leakage current compensation technique, CB, CS and BD compensation circuits can be used to further extend the temperature range of a Brokaw bandgap circuit. As described in Paper C, experiments were conducted to characterise a low power Brokaw bandgap temperature sensor and reference utilising different compensation techniques. For a full compensation scheme, the temperature sensors were seen to operate up to at least 230 °C at an average power consumption of 14 µW. Employing an 11-bit ADC, the sensor is able to operate an accuracy of 1 °C, provided that a multi-point digital calibration procedure is employed.

Q4: *What are critical design considerations and limitations for on-chip coils?*

The design considerations for on-chip coil design were studied in Papers D and F of this thesis. The loading of the coil was found to be a parameter of crucial importance and a limit for the load was found, beyond which the required transmitter power for a constant voltage generated at the load is not reduced even if the loading of the coil is decreased. This limit was found to lie around 10 kΩ for the process technology studied, where, according to simulations and measurements on manufactured devices, a power transfer efficiency of −43 dB is plausible. For a 10 kΩ load, the number of turns for the on-chip coil reaches a limit where it is no longer beneficial to increase the number of turns due to the adverse effects of the substrate and inter-turn capacitance. For higher-power designs, the amount of turns should be reduced and instead wider tracks should be prioritised.

In Paper F, it is recommended that for low-power operation, a single shunt capacitor is used as matching network due to the difficulty of manufacturing large inductors with high Q factors on-chip. However, it is important that the resonant circuit formed between

on-chip coil and on-chip capacitor is tuned to the transmitter frequency so that as much power as possible can be harvested. Paper E addresses this challenge by demonstrating a method for realising a high-Q trimmable capacitor on-chip. The trimming method is based on the blowing of fuses—in contrast to the switching of semiconductors—because semiconductors would require a DC bias in order to realise the desired trimming state, and a DC bias is not available at start-up of a single-chip wireless system.

6.2 Future Work

While the feasibility of an on-chip coil sensor system for condition monitoring of power semiconductors has been demonstrated, the current system design does not include all the necessary parts. Subsystems yet to be implemented include a high-temperature rectifier for harvesting the wirelessly transmitted energy from the reader coil, an ADC to sample the analogue voltage provided by the temperature sensor, a temperature-stable clock generator and a load modulator to transmit temperature data to an external coil. These components are necessary for a complete sensor system and would all need to be designed for low-power operation at high temperatures.

Furthermore, it is theorised in Paper A and Paper C that for a Brokaw bandgap reference, the negative effects of CB, SB and BD leakage current are mitigated by a high loop gain. It is possible that a circuit that yields a higher loop gain would further extend the temperature range of the sensor—or alternatively be used in place of the compensation circuits in order to save power.

While even higher temperatures are unlikely to be required for our application, a higher temperature range could nevertheless be interesting for other applications.

Because the simulation times for the gradient ascent algorithm used in Papers D and F of this thesis proved to be substantial, it is worth considering optimising it. Currently, some computation time is "wasted" on simulations of on-chip coil designs with a high number of turns for loads which will yield low power transfer efficiencies for more than a few turns. Furthermore, geometries with a high number of turns take significantly longer to simulate than do few-turn designs, exacerbating the problem. One way to reduce the amount of wasted time would be to start by examining a single-turn design, then proceed to a two-turn design. If the latter design proved to be better, then one more turn should be added and the procedure should be repeated. This procedure should continue until the power transfer efficiency for the coil design ceases to improve, for which case the best design thus far is chosen as the final design.

Chapter 7

Paper Summaries

In this chapter, summaries are provided for the papers from this thesis. The main work in Papers A–F was performed by the author of this thesis.

7.1 Paper A

Title: Leakage Current Compensation for a 450 nW, High-Temperature, Bandgap Temperature Sensor
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Published in: Proceedings of MIXDES 2015, 22nd International Conference "Mixed Design of Integrated Circuits and Systems"

In this paper, the theory of leakage current compensation circuits in Brokaw bandgap references is discussed. It is concluded that in addition to a previously known compensation technique which compensates for CS leakage, a CB and BD compensation circuit can be used to extend the temperature range of Brokaw bandgap sensors. The main idea of this compensation technique is to limit the net excess current entering the main bipolar pair to limit non-linearities introduced by leakage current. The theory is supported by circuit simulations.

7.2 Paper B

Title: Single Chip Wireless Condition Monitoring of Power Semiconductor Modules
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Published in: 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC)
This paper presents an assessment of the feasibility of on-chip coils for use in wireless temperature monitoring of power semiconductors in power semiconductor modules. A concept for such a monitoring scheme is presented and discussed in detail. An initial

attempt is presented at producing an on-chip coil for use in wireless temperature monitoring of power semiconductors. The self-capacitance of said coil was underestimated, resulting in low power transfer efficiencies. However, it is noted that earlier work in on-chip coil design exhibits higher power transfer efficiencies which are more suitable for our application.

7.3 Paper C

Title: High-Temperature Characterisation of Leakage Current Compensated, Low-Power, Bandgap Temperature Sensors
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Published in: Springer Analog Integrated Circuits and Signal Processing 2017

In this paper, en extensive experimental evaluation of the circuit introduced in Paper A is presented. A Brokaw bandgap reference is characterised for temperatures up to 230 °C. This characterisation is performed for circuits with no compensation, for circuits with CS compensation and for circuits with both CS compensation and CB/SB/BD compensation. It is found that depending on the accuracy requirements and which compensation circuits are used, the temperature range could be extended by 20 to 50 °C. Specifically, the CB/SB/BD compensation circuit was seen to prevent a certain type of malfunction from occurring, but reduces the accuracy slightly.

7.4 Paper D

Title: Chip-Coil Design for Wireless Power Transfer in Power Semiconductor Modules
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Published in: 2018 2nd Conference on PhD Research in Microelectronics and Electronics Latin America (PRIME-LA)

This paper presents simulations of coil geometries optimised for high power transfer efficiency for a PCB coil inductively coupled to an IC coil in a monitoring system for power semiconductor modules. A gradient-ascent algorithm based on earlier work is used to obtain the optimised geometries. Furthermore, the feasibility assessment initiated in Paper B is extended to include discussions on the loading of the on-chip coil as well as on the different parts of the power transfer efficiencies such as that of a power amplifier, the inductive link, matching networks and rectifier.

7.5 Paper E

Title: Maximal Q Factor for an On-Chip, Fuse-Based Trimmable Capacitor
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Published in: MDPI Electronics 2019

In order to address the challenge of on-chip frequency tuning for resonant circuits, this paper presents a method for realising a fuse-based trimmable on-chip capacitor. For the parallel capacitor bank topology studied, the method maximises the worst-case post-trim Q factor. Fuses are used as an alternative to switching semiconductors because they do not require a DC bias and are thus suitable for battery-free, single-chip wireless systems.

7.6 Paper F

Title: Load-Dependent Power Transfer Efficiency for On-Chip Coils
Authors: Joakim Nilsson, Johan Borg, Jonny Johansson
Submitted to: Springer Analog Integrated Circuits and Signal Processing 2019

In this paper, the loading of on-chip coils is studied in detail and a theoretical model for an on-chip coil with a single-capacitor matching network is developed. The theory is supported by gradient-ascent optimisations and electromagnetic simulations as well as measurements on manufactured devices. The optimisation algorithm is the same used in Paper D. The conclusion is drawn that for the system studied, there is a limit for the loading of the on-chip coil beyond which the transmitter power required to realise a constant load voltage is not reduced even if lighter loads are employed.

7.7 Papers not in Thesis

In this section, papers are listed that the author of this thesis has been part of, but that have not been included in the thesis.

Paper X1

Title: FPGA prototype of machine learning analog-to-feature converter for event-based succinct representation of signals
Authors: Sergio Martin del Campo Barraza, Kim Albertsson, Joakim Nilsson, Jens Eliasson, Fredrik Sandin
Published in: 2013 IEEE International Workshop on Machine Learning for Signal Processing (MLSP)

Paper X2

Title: A Feasibility Study of SOA-enabled Networked Rock Bolts
Authors: Jens Eliasson, Pablo Puñal Pereira, Henrik Mäkitaavola, Jerker Delsing Joakim Nilsson, Joakim Gebart
Published in: Proceedings of the 2014 IEEE Emerging Technology and Factory Automation (ETFA)

Paper X3

Title: Classifier Optimized for Resource-constrained Pervasive Systems and Energy-efficiency
Authors: Niklas Karvonen, Lara Lorna Jimenez, Miguel Gomez Simon, Joakim Nilsson
Published in: International Journal of Computational Intelligence Systems 2017

Paper X4

Title: Low-Power Classification using FPGA—An Approach based on Cellular Automata Neural Networks and Hyperdimensional Computing
Authors: Niklas Karvonen, Joakim Nilsson, Denis Kleyko, Lara Jimenez
Submitted to: 18th IEEE International Conference on Machine Learning and Applications

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Part II

Paper A

Leakage Current Compensation for a 450 nW, High-Temperature, Bandgap Temperature Sensor

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Leakage Current Compensation for a 450 nW, High-Temperature, Bandgap Temperature Sensor

Joakim Nilsson, Johan Borg and Jonny Johansson

Abstract

The design of a 450 nW bandgap temperature sensor in the 0 to 175 °C range is presented. The design demonstrates a leakage current compensation technique that is useful for low-power designs where transistor performance is limited. The technique mitigates the effects of leakage in Brokaw bandgap references by limiting the amount of excess current that is entering the bases of the main bipolar pair due to leakage. Using this technique, Monte Carlo simulations show an improvement factor of 7.6 for the variation of the temperature sensitivity over the full temperature range. For the variation of the reference voltage, Monte Carlo simulations show an improvement factor of 2.3.

Sensors built using this technique can be used to accurately monitor the temperature of power semiconductors since wireless temperature sensors become feasible with sufficiently low power consumption.

1 Introduction

In this work, the design of a low-power, high-temperature CMOS temperature sensor is presented. The target is to monitor the temperature of power semiconductors in order to predict failures of power electronic equipment. Many emerging power semiconductor faults, especially those related to the packaging of a device, manifest themselves as a temperature rise [1]. Thus, monitoring of temperature of a device can enable early fault detection and preventive maintenance. An example of a package fault is solder fatigue, where the solder that attaches the power semiconductor to its cooling base plate degenerates, resulting in reduced cooling efficiency [2].

Monitoring of high power devices can be challenging as the operating range is often specified to high temperatures. Such high temperatures introduce non-linearities in standard temperature sensors due to leakage currents in hot parasitic reverse-biased p-n junctions. These currents increase exponentially with temperature, making them particularly difficult to deal with in high-temperature applications. Methods exist to compensate for the effects of leakage currents [3–5], but additional compensation may be required when low-power sensors are operated at high temperatures.

Due to challenges with galvanic isolation, high voltages in power semiconductors complicate the process of measuring die temperature. For this reason, indirect measurement methods have been developed [1]. Three such methods were demonstrated in [6], where different parameters were measured and used to estimate the junction temperature of a

power MOSFET device. Drawbacks of these indirect approaches are that much must be known about the device to measure on and that the obtained measurements may not be as accurate as direct measurements would be.

Using wireless technology, challenges with galvanic isolation can be avoided. The limited amount of power available in a wireless sensor places stringent demand on its power consumption. Low-power operation at high temperatures is particularly challenging since leakage currents increase exponentially with temperature and become a serious problem when their magnitude approaches that of the circuit's quiescent current.

This paper presents the design and simulations of a 450 nW CMOS chip for the generation of a proportional to absolute temperature (PTAT) voltage as well as a stable bandgap reference voltage in the 0 to 175 °C range. The circuit incorporates a leakage current compensation technique, where a Brokaw bandgap reference [7] is used as a base, and focus is put on combining high-temperature measurements with low-power operation. In particular, the effects of leakage current are studied and leakage current compensation techniques are discussed and simulated. The results will be used as a base in the design of a wireless temperature measurement system for power semiconductors.

In Section 2, this paper presents an overview of the operation of the Brokaw bandgap reference. Emphasis is put on how leakage currents affect circuit operation and how previous work has compensated for leakage currents. In Section 3, a circuit is presented to demonstrate a leakage current compensation technique. In Section 4, simulation results of said circuit are presented with discussions in Section 5. Conclusions are presented in Section 6.

2 The Brokaw Bandgap Reference

The Brokaw bandgap reference [7], an implementation of which is depicted in Figure 1, is a commonly used circuit for accurately measuring temperature or for providing a temperature insensitive bandgap voltage. It operates by having MOS transistors M_3, M_4, and M_5 enforce equal collector currents, I_{C1} and I_{C2}, through the bipolar pair, Q_1 and Q_2, while relying on differently sized emitter areas to produce a PTAT voltage, V_{PTAT}, over resistance R_2 and a temperature-independent reference voltage, V_{REF}, at the bases of the bipolar pair. V_{REF} is the result of the summation of V_{PTAT} and the complementary to absolute temperature (CTAT) base-emitter (BE) voltage of Q_1, V_{BE1}. In order for V_{REF} to be temperature insensitive, $\partial V_{\mathrm{PTAT}}/\partial T$, which is positive, must be controlled so that it cancels out $\partial V_{BE1}/\partial T$, which is negative. This can be done by adjusting the ratio between the resistances R_1 and R_2.

2.1 Leakage Currents in Brokaw Bandgap References

Leakage currents in reverse-biased p-n junctions increase exponentially with temperature. This introduces challenges for circuit designers who design for the high temperature range. A particular challenge with the Brokaw bandgap reference is that the collector-substrate (CS) leakage currents of Q_1 and Q_2 differ in magnitude due to differing transistor sizes.

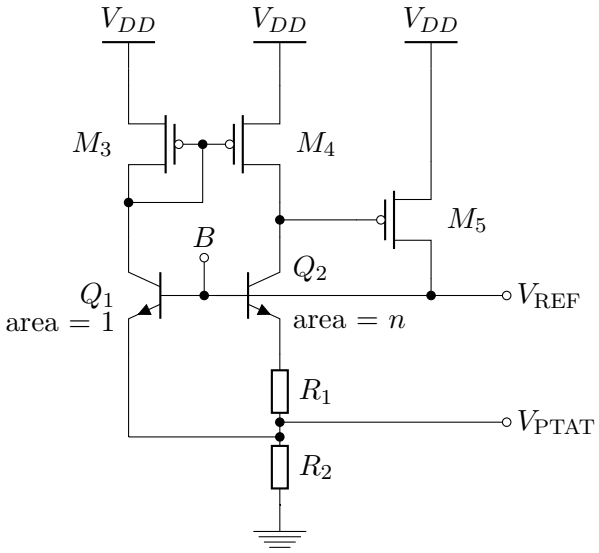

Figure 1: Brokaw bandgap reference circuit. For simplicity, the start-up circuit has been omitted.

This size mismatch results in a mismatch in collector currents. Since an essential part in proper circuit operation is the assumption of equal collector currents, leakage currents will cause V_{PTAT} to become less linear at high temperatures. This non-linearity will also be present in V_{REF}, since V_{REF} is the sum of V_{PTAT} and V_{BE1}.

2.2 Earlier Work in Leakage Current Compensation Techniques

To mitigate the effects of leakage currents in bandgap circuits, Radoiaş et al. introduced a leakage current compensation technique in 2012 and used it to produce a Widlar bandgap circuit [8] with improved temperature dependence [4]. In 2013, the same group used said technique to improve the temperature dependence of a Brokaw bandgap circuit [5].

The latter circuit introduced an additional transistor having a shorted BE junction connected to the emitter of Q_1 and its collector to the collector of Q_1. In this way, the new transistor is operated in cut-off mode and therefore does not affect circuit operation, but is still under the effect of the same CS leakage current phenomenon as are Q_1 and Q_2. If the emitter area of the new transistor equals the difference between the emitter areas of Q_1 and Q_2, then the leakage current from the collector nodes roughly match, and the only remaining mismatches are those which result from mismatches in device parameters and reverse-voltages. This technique has the effect that it reduces the magnitude of the non-linearities resulting from mismatches in collector currents.

2.3 Leakage-Induced Excess Base Current

In the works referenced in Section 2.2, Radoiaş et al. do not mention any effect that the leakage of the reverse-biased collector-base (CB) junctions of Q_1 and Q_2 or the reverse-biased body-drain (BD) junction of M_5 have on circuit operation, nor do they compensate

for such leakage. A non-linearity, which is the main topic of this work, can result from the leakage currents produced from said junctions. These leakages cause excess current to be introduced at the bases of the bipolar pair, node B. Leakage introduced at node B has a particularly severe effect on circuit operation since any excess current introduced there is amplified by the bipolar transistors.

Assume that the collector current of Q_1, I_{C1}, changes due to CB or BD leakage and current amplification in Q_1. This change in current will change the voltage at the collector of Q_2 due to the current mirror action of M_3 and M_4. That voltage signal will in turn be amplified by the common source amplifier, M_5. The majority of the change in output current from M_5 will take the path through the BE junction of Q_1 since that path has lower impedance than the path through the BE junction of Q_2, since Q_1 is biased at a higher current density and has no series resistor. This current will be amplified by Q_1 and counteract the initially assumed change of I_{C1}. Neglecting the Early effect of Q_2, the loop gain along the feedback path, A_L, is proportional to $r_{o4}g_{m5}\beta_1$, where r_{o4} is the small signal output resistance of M_4, g_{m5} is the small signal transconductance of M_5, and β_1 is the current gain of Q_1. It is a challenge to achieve high loop gain for low power designs since all variables in the expression for A_L benefit from higher power levels.

If A_L is not high enough, a change in I_{C1} is not reduced to a negligible amount and the currents I_{C1} and I_{C2} will not be equal. Therefore, the assumption made in the beginning of this section about equal collector currents no longer holds, resulting in non-linearities being introduced in the output voltages V_{REF} and V_{PTAT}.

3 Circuit Design

To compensate for excess current leaking into node B in Figure 1, a source of artificial leakage current can be introduced, leaking out the same amount of current from the node that is leaking into it. This can be achieved with a current mirror and cut-off transistors with dimensions equal to those of Q_1, Q_2 and M_5. The purpose of the cut-off transistors is to replicate the leakage current of the ordinary transistors.

3.1 Proposed Circuit

In 1998, Mizuno et al. [3] proposed a technique to create a source of artificial leakage current. This technique takes into account differences in reverse-voltages between p-n junctions in replicas and ordinary transistors, resulting in better matching between original and artificial leakage currents compared to only using a current mirror. In this work, we apply the technique of Mizuno et al. to minimise the net excess current entering node B due to leakage. Specifically, replicas of transistors Q_1, Q_2 and M_5 are added and used as input to a PMOS version of the precise circuit from [3], the output of which is connected to node B. The resulting circuit is depicted in Figure 2. The bipolar replicas, Q_1', Q_2', Q_1'' and Q_2'' are made to operate in cut-off mode by connecting their collectors to V_{DD} while shorting their BE junctions and connecting them to the compensation circuit. The MOSFET replica, M_5', is made to operate in cut-off mode by connecting its gate

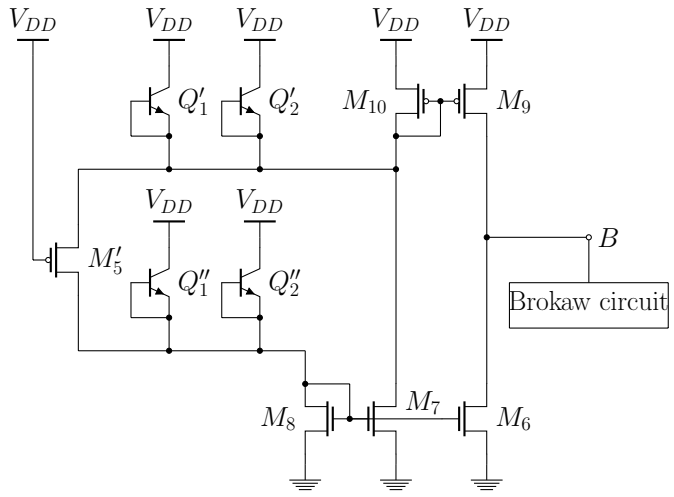

Figure 2: Compensation circuit connected to the Brokaw bandgap circuit from Figure 1. The prim/bis notation denotes devices identical to similarly named devices from the Brokaw bandgap circuit depicted in Figure 1. Figure corrected after publication.

Table 1: Dimensions of transistors from the circuits of Figure 1 and Figure 2 for a 0.18 µm *design.*

Device		
MOSFETs	*width* [nm]	*length* [nm]
M_3, M_4	2000	360
M_5	2000	720
M_6, M_7, M_8, M_9, M_{10}	2000	3600
BJTs	*emitter area* [µm^2]	
Q_1	6.8	
Q_2	40.8	

to V_{DD} while connecting its drain and source to the compensation circuit. Two sets of replicas are needed for the bipolar transistors since the compensation circuit operates by measuring the leakage current produced by two p-n junctions. This is not the case for the MOSFET replica, as both its source and drain can be used as input to the compensation circuit.

3.2 Transistor Dimensions

For a 0.18 µm design, transistor dimensions from the circuits of Figure 1 and Figure 2 are summarised in Table 1.

In order to minimise leakage current, transistor widths for MOSFETs should be small

since that results in smaller areas of reverse-biased BD junctions. On the other hand, small width increases the overdrive voltage for a given drain current, which increases the required supply voltage and therefore the power consumption. As a compromise between these two constraints, all MOSFETs have a width of 2 µm.

A short length of the mirroring transistors M_3 and M_4 reduces the output resistance of the current mirror, lowering the loop gain, A_L. A long length would increase the overdrive voltage of said transistors, increasing required supply voltage. As a compromise between these two constraints, M_3 and M_4 have a length of 360 nm.

Matching collector voltages of Q_1 and Q_2 allows for better matching of leakage currents for the compensation technique of Radoiaş et al. [5] due to matching reverse voltages over CS junctions. Good matching of collector voltages can be achieved if the length of M_5 is increased compared to M_3 and M_4. M_5 has a smaller drain current and therefore requires longer length for the same gate voltage. Because of smaller drain current, the overdrive voltage of M_5 does not increase the required supply voltage for sufficiently short length such as 720 nm as used in this design.

For transistors M_6, M_7, M_8, M_9, and M_{10} in the compensation circuit of Figure 2, a higher overdrive voltage than for M_3, M_4, and M_5 can be afforded since the full supply voltage is available to them. A longer length results in higher output resistance and therefore better leakage current matching. Those transistors have a length of 3.6 µm.

The emitter area of Q_1 is of the minimum size available in the process library, 6.8 µm^2. In accordance with common practice in bandgap circuit design, the emitter area of Q_2 is 6 times that size, 40.8 µm^2.

4 Simulation Results

A chip design was created in a 0.18 µm process, based on the circuit described in Section 3. All bipolar devices were implemented using vertical bipolar junction transistors. Parasitics were extracted from the design and simulations of the resulting circuit were run.

For both the compensated and uncompensated circuits from Figure 2 and Figure 1, respectively, Figure 3 shows a plot of the reference voltage, V_{REF}, as a function of temperature. It can be seen that the uncompensated voltage increases exponentially for high temperatures, whereas the compensated voltage is affected only marginally even in the high-temperature range. Over the full temperature range, V_{REF} varies 17.1 mV for the uncompensated circuit, compared to 1.9 mV for the compensated circuit.

In Figure 4, a similar plot is shown for the temperature sensitivity of the PTAT voltage, $\partial V_{\mathrm{PTAT}}/\partial T$. For the high-temperature range, an observation similar to the one made for V_{REF} can be made for $\partial V_{\mathrm{PTAT}}/\partial T$, but in this plot, the non-linearity for the compensated circuit is more clearly visible. Over the full temperature range, $\partial V_{\mathrm{PTAT}}/\partial T$ varies 1.66 mV/°C for the uncompensated circuit, compared to 243 µV/°C for the compensated circuit.

For the compensated circuit, a plot of the power consumption as a function of operating temperature is shown in Figure 5. It can be seen that for low temperatures the

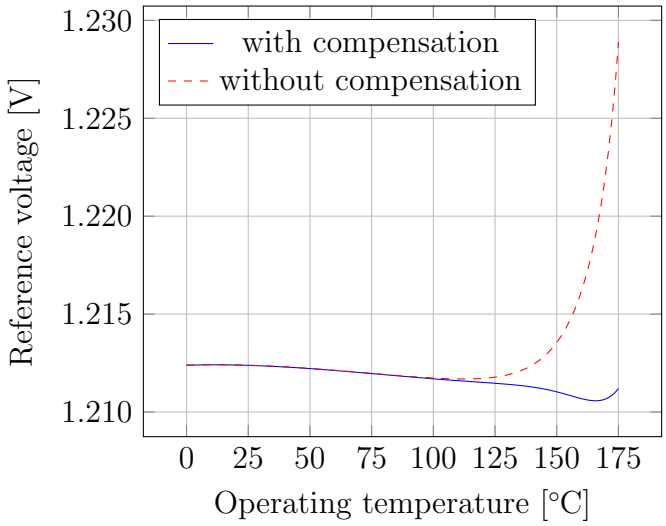

Figure 3: Simulation result of the reference voltage, V_{REF}, as a function of operating temperature for a Brokaw bandgap reference (Figure 1) with and without compensation circuit (Figure 2).

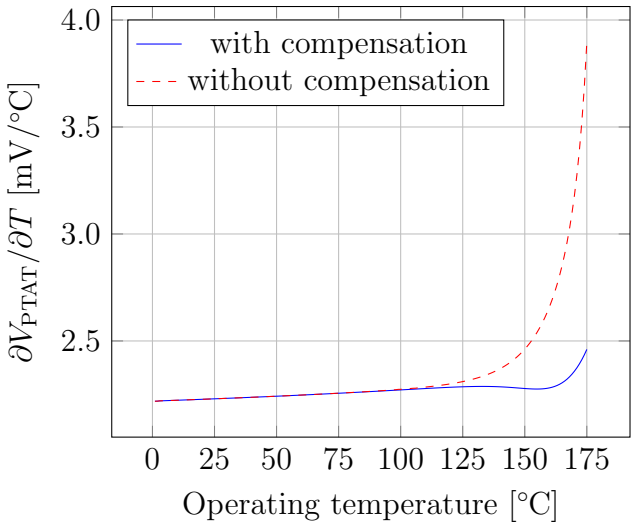

Figure 4: Simulation result of the temperature sensitivity of the PTAT voltage, $\partial V_{PTAT}/\partial T$, as a function of operating temperature for a Brokaw bandgap reference (Figure 1) with and without compensation circuit (Figure 2).

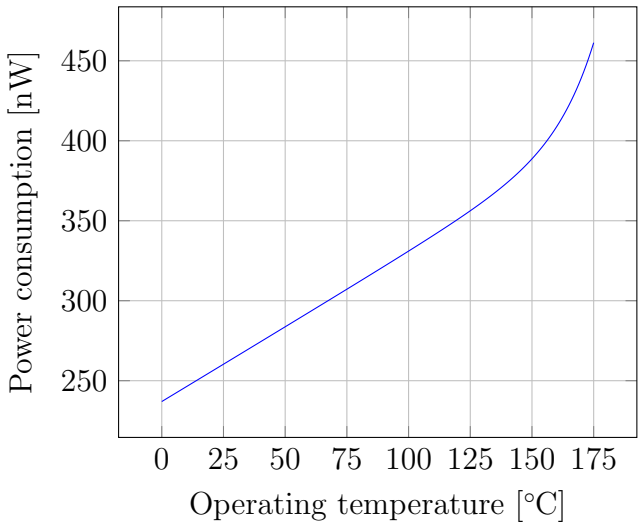

Figure 5: Simulation result of the power consumption as a function of operating temperature for a Brokaw bandgap reference (Figure 1) with compensation circuit (Figure 2). The circuit was operated with a power supply of 2 V.

power consumption is a linear function of temperature, while for high temperatures a superimposed exponential component is seen.

Main performance parameters for both compensated and uncompensated circuits extracted from Monte Carlo simulations are summarised in Table 2. From the table, it can be seen that adding the compensation circuit does not adversely affect the accuracy of the reference voltage or the temperature sensitivity.

5 Discussion

In this section, various aspects of the proposed circuit are analysed and compared with other work.

5.1 Compensation Circuit Power Consumption

The compensation circuit consumes current of the same order of magnitude as the current it is compensating for. Therefore, a small increase in power consumption could be expected for high temperatures. If there is such an increase, it is too small to be significant for the Monte Carlo simulations performed in this work, as no significant difference in power consumption can be seen in Table 2 between the compensated and uncompensated cases.

Table 2: Summary of parameters obtained from a 100*-sample Monte Carlo simulation of both compensated and uncompensated circuits. 'Average value' is the average taken over the full temperature range. 'Max/min variation' is the difference between the maximum and minimum values in the full temperature range. Values for the power consumption are given for a power supply of* 2 V.

Parameter	**Uncompensated**		**Compensated**	
Reference voltage	*mean*	*std. dev.*	*mean*	*std. dev.*
Average value [V]	1.227	0.1054	1.213	0.0987
Max/min variation [mV]	21.95	6.892	9.430	6.847
$\partial V_{\mathrm{PTAT}}/\partial T$	*mean*	*std. dev.*	*mean*	*std. dev.*
Average value [mV/°C]	2.360	0.061 30	2.254	0.058 43
Max/min variation [µV/°C]	1950	808.2	258.2	67.39
Power consumption [nW]	*mean*	*std. dev.*	*mean*	*std. dev.*
at 27 °C	264.8	30.94	262.4	32.64
at 175 °C	441.1	35.07	438.9	36.40

5.2 Total Power Consumption Characterisation

As can be seen in Figure 5, for low temperatures, the total power consumption, P_{TOT}, is a linear function of temperature, but increases more rapidly for higher temperatures. This behaviour can be explained by realising that P_{TOT} consists of two main parts, P_Q and P_{LEAK}. P_Q is the power consumed due to the quiescent current, I_Q, used to bias transistors Q_1 and Q_2, while P_{LEAK} is the power consumed by leakage currents and the compensation.

The quiescent current, I_Q, is determined by resistor R_2. Since the voltage over R_2, V_{PTAT}, is proportional to absolute temperature, the current through it, $I_2 = I_Q$, is also proportional to absolute temperature, $I_Q \propto T$. I_Q is supplied by V_{DD}, so the power consumption resulting from it, P_Q, equals $I_Q \cdot V_{DD}$. Therefore, assuming V_{DD} is constant, $P_Q \propto T$.

The total amount of leakage current, I_{LEAK}, is exponentially related to temperature. Under the assumption that leaked current does not change the voltages over which it is leaking, P_{LEAK} will be proportional to I_{LEAK}, hence $P_{\mathrm{LEAK}} \propto e^T$.

Since the magnitude of the leakage current is small for low temperatures, P_Q will dominate the power consumption in the low temperature range while, for high temperatures, P_{LEAK} can contribute significantly. Therefore, attempting to reduce I_Q below a certain value in order to decrease power consumption will be ineffective for the high-temperature range.

5.3 Comparison with Other Work

At higher power levels other works have demonstrated results similar to the results of this work. An example is [4], where the same temperature range as in this work was achieved, but with at least 10 times the power consumption.

Sensors that achieve higher operating temperatures do so with further increased power consumption. For example, [9] is characterised up to 225 °C at a power consumption of 112.5 µW, while [10] is characterised up to 200 °C at a power consumption of 40 µW. Both of these sensors were fabricated in silicon on insulator (SOI) processes, for which high-temperature design is facilitated due to lower leakage currents. SOI-technology could be used to further extend the temperature range of the sensor presented in this work.

The authors are not aware of bandgap circuits that achieve lower power consumption than the sensor presented in this work, neither are they aware of sensors using other topologies that achieve lower power consumption and are characterised in the same high-temperature range as the sensor from this work. Two examples that achieve lower power consumption include [11] and [12], which are only characterised up to 100 °C and 60 °C, respectively.

6 Conclusion

A leakage current compensation circuit [3] is used in a Brokaw bandgap circuit in order to minimise the net amount of excess current leaking into the bases of its main bipolar transistors. This results in improved linearity with respect to temperature for the reference voltage and the PTAT voltage. The technique is useful for circuits whose devices have low gain, e.g. low-power circuits, and can be used to extend the operating temperature range of bandgap temperature sensors or bandgap references.

For the bandgap circuit depicted in Figure 1, simulation results over the 0 to 175 °C temperature range show that the variation of the reference voltage was improved from 17.1 mV to 1.9 mV, while the variation of the temperature sensitivity was improved from 1.66 mV/°C to 243 µV/°C when the compensation circuit from Figure 2 was added.

The technique will be used to enable accurate condition monitoring of power semiconductor devices through wireless power and data transfer.

Acknowledgement

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Paper B

Single Chip Wireless Condition Monitoring of Power Semiconductor Modules

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Single Chip Wireless Condition Monitoring of Power Semiconductor Modules

Joakim Nilsson, Johan Borg and Jonny Johansson

Abstract

A concept for doing accurate monitoring of temperature in power semiconductor modules is proposed. The concept involves glueing wireless single-chip temperature sensors with on-chip coils in direct contact with power semiconductor devices within their modules. Direct contact results in accurate temperature measurements while wireless technology such as RFID provides galvanic isolation from the power devices.

An overview of the electromagnetic situation within wire bond power semiconductor modules is presented and a prototype chip with an on-chip coil has been manufactured as an initial attempt to investigate the feasibility of the concept. Measurements on said chip provides some insight in the challenges in on-chip coil designs.

The feasibility of the concept is supported by earlier work that have demonstrated high power transfer efficiencies and a low power temperature sensor that is able to operate at high temperatures.

1 Introduction

A study conducted in 2007 shows that 34 % of failures occurring in power electronic equipment are due to solder faults or faults in semiconductors [1]. Condition monitoring of power semiconductors can be used to predict such failures so that scheduled maintenance can be performed and catastrophic or secondary failures can be avoided. A rise in temperature can be an indication of an emerging fault and two studies suggest that monitoring of the power semiconductor temperature is a promising method for predicting emerging failures [2, 3].

This paper presents the idea of using wireless direct contact temperature sensors for use in condition monitoring of power semiconductors. Such sensors could make emerging faults in power semiconductors easier to predict by providing accurate measurements of temperature. This is especially true for faults related to the packaging of a device. A common package fault is solder fatigue, where the solder that attaches the power semiconductor to its cooling base plate degenerates, reducing the cooling efficiency which eventually results in the device becoming permanently damaged due to overheating [4].

A wireless approach solves the problem of providing galvanic isolation from the power semiconductor. Another approach is to take indirect measurements to provide galvanic isolation. Three indirect methods were demonstrated in [5] that estimate the junction temperature of a power MOSFET device by taking measurements of its various voltages

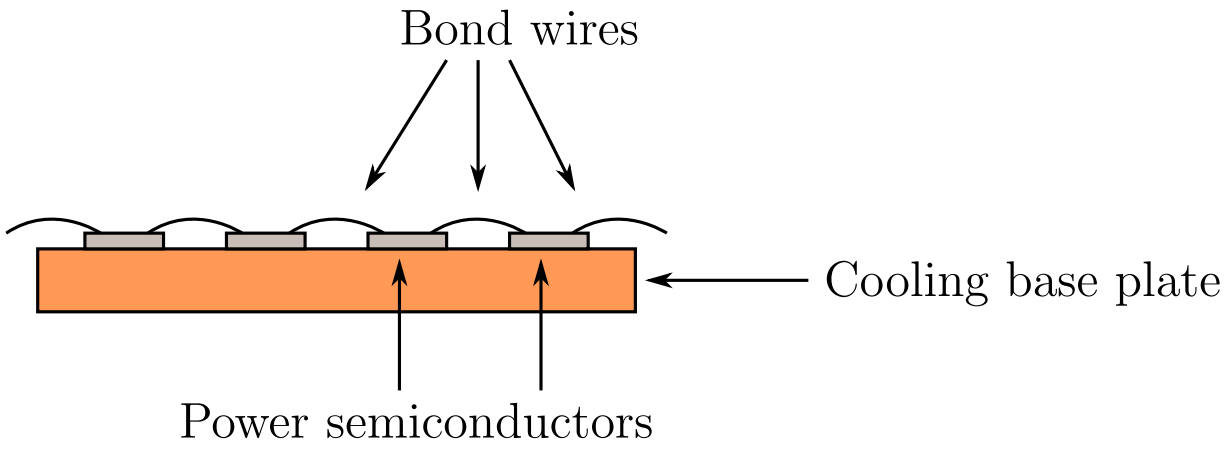

Figure 1: Schematic view of the cross-section of a wire-bond power semiconductor module.

and currents and calculating the estimated temperature from them. Drawbacks of these methods are increased system complexity and increased level of required understanding for the same accuracy.

In this work, we propose wireless, low power, single chip temperature sensors with on-chip coils as a solution for performing condition monitoring on power semiconductors. For this type of sensor, the on-chip coil is a critical component. As demonstrated by Zargham and Gulak[1], it is possible to achieve good power transfer efficiency from an external reader to a carefully designed on-chip coil [6]. An initial attempt at producing a prototype on-chip coil is demonstrated in this work, and experiments performed on it provides some insight in problems that can arise.

The paper is organised as follows. In Section 2 the concept of wireless monitoring of temperature for power semiconductors is described. Section 3 describes experiments on a prototype coil with results in Section 4. A discussion of the results are presented in Section 5 and the paper is concluded in Section 6.

2 Wireless Temperature Measurement in Power Semiconductor Modules

Shown in Figure 1 is an illustration of the cross-section of a wire-bond power semiconductor module, which is the focus of this work. Other types of modules, such as the press pack module [7], are not considered in this work.

The base in a wire-bond power semiconductor module is a ceramic substrate, called the base plate, onto which power semiconductors are soldered. One purpose of the base plate is to cool the power semiconductors. A metal plate in contact with the base plate is usually exposed at the bottom of the module so that it can be mounted on a heat sink.

To be able to accurately monitor the temperature of a power semiconductor device while providing galvanic isolation, we propose glueing a single-chip sensor directly onto

[1]Names corrected after publication.

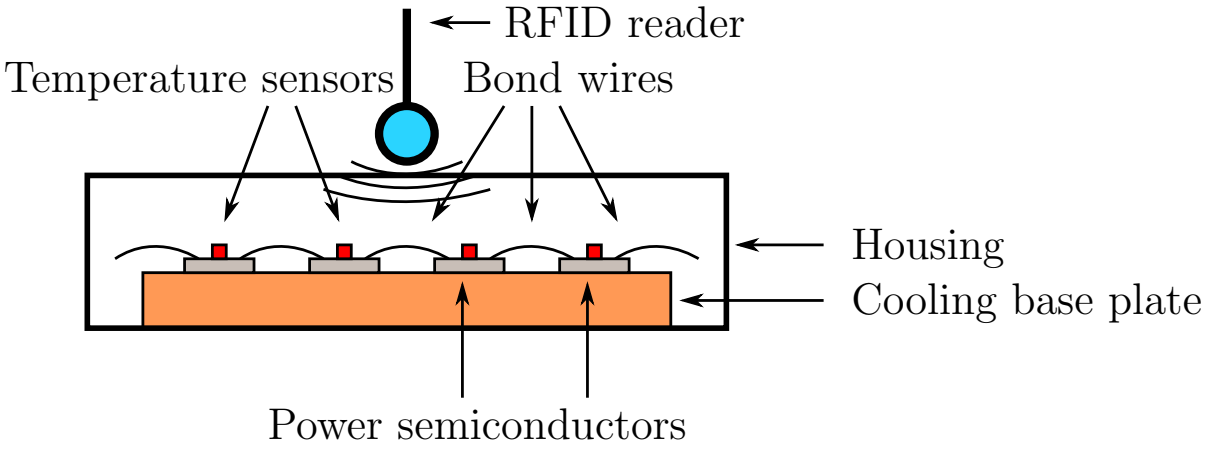

Figure 2: Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by a nearby RFID reader.

power semiconductors and communicate to the sensor through a wireless technology such as radio-frequency identification (RFID). The concept is illustrated in Figure 2 and requires the sensor chip to include an on-chip coil. The small size and lack of electrical connections of an integrated circuit with on-chip coil enable multiple sensors to be glued onto a single power semiconductor. This enables measurements of the spatial distribution of temperature over the power semiconductor, which could make faults such as solder fatigue easier to predict as compared to measuring the temperature at a single point on the power device.

There are several options for the placement of the reader coil. In Figure 2, the reader is mounted on the outside of the module housing. This enables easy integration of the coil with existing modules since no modifications need to be made inside the module except for adding temperature sensors which do not require any extra wires. Another advantage is that the reader coil can be easily aligned the with on-chip coils of the sensors. Such a coil could either be a wire wound coil or a printed circuit board (PCB) coil. Another possibility is to integrate the coil within the power semiconductor module. While this approach requires some modification to existing modules, it has the advantage of closer distance between reader and sensor. Depending on the dimensions of the module, this approach may be necessary to achieve a sufficiently high power transfer efficiency between reader and temperature sensors.

There are several aspects that affect the electromagnetic situation. These include:

1. The substrate of the sensor chip. Currents induced in the substrate reduce the strength of transmitted signals.

2. The power semiconductor. Currents induced in he substrate of the power semiconductor reduce the strength of transmitted signals. In addition to this, the on and off switching of currents typically present in power semiconductors produce strong electromagnetic fields that may disturb the communication between reader

and sensor.

3. The base plate. Currents induced in the base plate reduce the strength of transmitted signals.

4. The spatial separation between sensor and reader. A larger distance between reader and sensor reduces the power transfer efficiency. This distance is determined by the dimensions of the power semiconductor module and the positioning of the reader coil.

Since power semiconductors are commonly operated at high temperatures and since power is supplied wirelessly for this type of monitoring, the concept requires high temperature, low power temperature sensors such as the sub-µW sensor demonstrated in [8].

Although the electromagnetic environment in a power semiconductor module is complex, an indication of the feasibility can be seen from works on-chip coils in other environments. For example, in a work on implantable chips in humans, wireless transfer efficiencies in air of better than 1 % at a distance of 10 mm have been demonstrated [6] and its 2.18 mm × 2.18 mm on-chip coil could be used in conjunction with the 450 nW sensor from [8] to implement the condition monitoring scheme proposed in this work.

3 On-chip Coil Protoype

In contrast to [6] where power levels in the range of 1 to 10 mW were achieved, we foresee significantly lower power requirements in our applications. As demonstrated in [8], accurate temperature sensors consuming as little as 450 nW are possible to implement. However, to leave some margin for other on-chip circuits such as A/D conversion, communication and control circuits, our first attempt at building an on-chip coil targeted a total power budget of 40 µA at 2 V, or 80 µW. The intended operating frequency of this prototype was 13.56 MHz, which is often used for RFID applications. As we found it to be impossible to build an on-chip coil with any significant Q-value for this frequency, the coil was instead optimised so that the resistance of the coil approximately matches the load impedance (2 V / 40 µA = 50 kΩ) of the on-chip circuits. The result was a 1.525 mm × 1.525 mm square coil with 199 turns and an inductance of approximately 150 µH (X_L = 12.8 kΩ, Q = 0.26). As our intended operating frequency is significantly lower than that used in [6] (187 MHz[2]), significantly lower power transfer efficiency can be expected. The coil was manufactured in 180 nm CMOS with no special post-processing steps carried out to manufacture the coil. Such post-processing can be used in order to produce higher quality coils by for example electroplating a Cu winding and a NiFe core onto a semiconductor chip [9], but this work focuses instead on cheaper coils that do not require such processing.

The remainder of this section describes two experiments that were performed on this prototype chip coil. A schematic of the experiment setup is shown in Figure 3.

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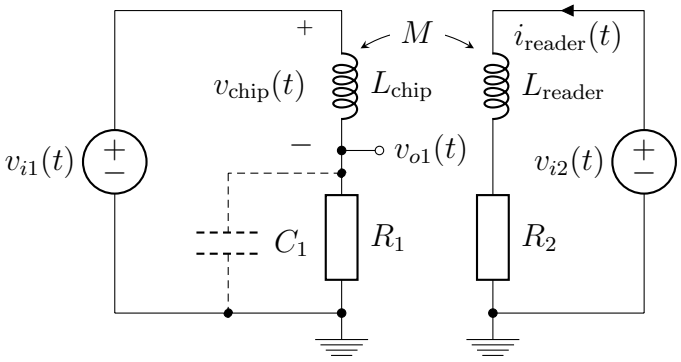

Figure 3: Schematic of the experiment setup. The left-hand side represents the chip coil, L_{chip} connected in series with the resistor R_1 and the signal generator $v_{i1}(t)$. The right-hand side represents the reader coil, L_{reader}, coupled to the chip coil, L_{chip}, with mutual inductance, M and connected in series with the resistor R_2 and the signal generator, $v_{i2}(t)$. C_1 represents the stray capacitance caused by the circuit board and the measurment equipment.

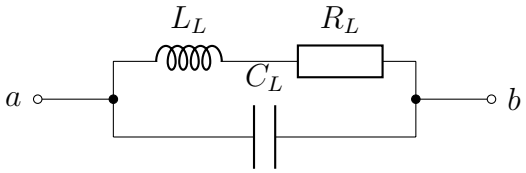

Figure 4: Equivalent model for a coil inductor.

L_{chip} represents the on-chip coil, while L_{reader} represents the reader coil. Actual power semiconductor chips were not included in this setup.

3.1 Chip coil parameter estimation

The left-hand part of the circuit shown in Figure 3 was used for this experiment. A frequency sweep of the voltage, $v_{i1}(t)$, was performed and the resulting waveforms, $v_{i1}(t)$ and $v_{o1}(t)$, were sampled. A Fourier transform was taken on the acquired samples to obtain the phasors $\mathbf{V_{i1}}(j\omega)$ and $\mathbf{V_{o1}}(j\omega)$. From the schematic shown in Figure 3 with the model of the coil inductor shown in Figure 4 replacing L_{chip} and taking into account stray capacitance, C_1, in parallel with R_1, the voltage division from $\mathbf{V_{i1}}(j\omega)$ to $\mathbf{V_{o1}}(j\omega)$ yields

$$\frac{\mathbf{V_{o1}}(\mathrm{j}\omega)}{\mathbf{V_{i1}}(\mathrm{j}\omega)} = \frac{Z_1}{Z_1 + Z_{\text{chip}}}, \tag{1}$$

where

$$Z_1 = R_1 \parallel \frac{1}{\mathrm{j}\omega C_1},$$

and

$$Z_{\text{chip}} = (R_{L_{\text{chip}}} + \mathrm{j}\omega L_{L_{\text{chip}}}) \parallel \frac{1}{\mathrm{j}\omega C_{L_{\text{chip}}}}.$$

Table 1: Specifications for the reader coil used in this work.

Paremeter	Value
Wire material	Copper
Wire diameter	0.3 mm
Coil diameter	10 mm
Coil height	8 mm
Number of turns	25

Taking the real and imaginary parts on both sides of Eq. (1) produces two new equations which were used with the sampled data in a Gauss-Newton optimiser to obtain estimates of the coil parameters $R_{L_{\text{chip}}}$, $L_{L_{\text{chip}}}$ and $C_{L_{\text{chip}}}$.

3.2 Power transfer efficiency

To assess the power transfer efficiency from an external coil to the chip coil, a reader coil was manufactured according to the specifications given in Table 1. The separation between reader coil and chip coil was set to 7 mm. Consider the circuit shown in Figure 3. The voltage source $v_{i1}(t)$ and the resistor R_1 were replaced by open circuits and the induced voltage, $v_{\text{chip}}(t)$, over L_{chip} was measured for different frequencies on the voltage source $v_{i2}(t)$. The current, $i_{\text{reader}}(t)$, through the reader coil was also monitored by measuring the voltage over resistor R_2.

If the reader circuit is implemented as a resonant circuit driven by a power amplifier, the dominant resistance is that of the reader coil, $R_{L_{\text{reader}}}$, and the losses in the reader will be given by:

$$P_{\text{loss}} = I^2_{\text{reader, rms}} R_{L_{\text{reader}}}, \tag{2}$$

where $I_{\text{reader, rms}}$ is the root-mean-square (rms) current passing through the reader coil.

The maximum achievable power transferred to a circuit connected to the chip coil occurs when the resistance of that circuit is matched to that of the resistance of the chip coil, $R_{L_{\text{chip}}}$. This power is given by:

$$P_{\text{useful}} = \frac{V^2_{\text{chip, rms}}}{4R_{L_{\text{chip}}}}, \tag{3}$$

where $V_{\text{chip, rms}}$ is the rms value of the voltage induced in the reader coil, L_{reader}. Combining Eq. (2) and Eq. (3) yields

$$\eta_{\max} = \frac{P_{\text{useful}}}{P_{\text{loss}}} = \frac{1}{4R_{L_{\text{reader}}} R_{L_{\text{chip}}}} \frac{V^2_{\text{chip, rms}}}{I^2_{\text{reader, rms}}}, \tag{4}$$

where $\eta_{\max}$ is the power transfer efficiency with matched load resistance.

Table 2: Measured and calculated data for the power transfer experiment efficiency described in Section 3.2. $I_{reader,\ rms}$ and $V_{chip,\ rms}$ are the observed amplidudes of the reader coil current and the chip coil voltage, respectively. η_{max} is the calculated power transfer efficiency based on the measurements and estimations for the coil resistances.

Paremeter		
Frequency	125 kHz	1 MHz
Measured parameters		
$I_{\text{reader, rms}}$	62.9 mA	16.7 mA
$V_{\text{chip, rms}}$	3.85 mV	6.20 mV
Calculated parameters		
η_{max}	0.222 ppm	8.22 ppm

4 Results

Based on the data obtained from the experiment presented in Section 3.1 with two frequency sweeps from 10 kHz to 1 MHz for both $R_1 = 1\,\text{k}\Omega$ and $R_1 = 47\,\text{k}\Omega$, estimations of the inductor parameters, $R_{L_{\text{chip}}}$ and $C_{L_{\text{chip}}}$, were found to be 47.6 kΩ and 3.42 pF, respectively. Gauss-Newton optimisation did not show stable values for the inductance, $L_{L_{\text{chip}}}$, and a closer examination of the data revealed that the circuit showed no significant inductive behaviour. The reason for this is the high values of $R_{L_{\text{chip}}}$ and $C_{L_{\text{chip}}}$. At high frequencies where the inductive part of the impedance starts to become significant compared to the resistance $R_{L_{\text{chip}}}$ the capacitive part becomes dominant and makes the coil act as a short circuit, hindering any efforts to measure the inductance. Electromagnetic simulations support this argumentation by showing a simulated inductance of 150 µH which is small enough compared to the obtained capacitance and resistance that the whole circuit does not show any significant inductive behaviour.

Data for two frequencies were obtained from the experiment presented in Section 3.2 with a reader-chip separation of 7 mm. This data is summarised in Table 2. Measurements at higher frequencies were complicated by the capacitive coupling of the reader coil to the measurement PCB and the obtained data for those frequencies was therefore excluded. It is possible that the effect of capacitive coupling is present in the measurement results also for the lower frequencies and therefore a more precise experiment setup would be beneficial. Table 2 includes calculated values, using Eq. (4), for the power transfer efficiency, η_{max}, based on the measured voltages and currents, $I_{\text{reader, rms}}$ and $V_{\text{chip, rms}}$ along with estimations of $R_{L_{\text{chip}}}$ and $R_{L_{\text{reader}}}$. $R_{L_{\text{chip}}}$ was found to be 45.1 kΩ through the chip coil parameter estimation process described in earlier in this section, while $R_{L_{\text{reader}}}$ was calculated to be 187 mΩ from the specifications of the reader coil, shown in Table 1.

5 Discussion

Based on a simulated coil inductance of 150 µH, a total coil impedance 47.6 kΩ+j12.8 kΩ results. Hence, the large self capacitance of 3.42 pF is clearly much too large for operation at 13.56 MHz as it corresponds to a reactance of about 3.4 kΩ. Thus, a large fraction of the induced voltage would be lost due to the voltage division between $R_{L_{\text{chip}}} + L_{L_{\text{chip}}}$ and $C_{L_{\text{chip}}}$. Considering the behaviour of the power transfer efficiency, η_{max}, Table II shows that when increasing the frequency from 125 kHz to 1 MHz, η_{max} increases by a factor 37.0. This differs from the theoretical value for ideal coils of $8^2 = 64$ (since the frequency was increased by a factor of 8), again possibly due to voltage division when driving the large self-capacitance. Taking this into account, the theoretical improvement from 125 kHz to 1 MHz was calculated to be a factor 46, in closer agreement with the measured value.

Optimising the coil to match the load impedance without considering the self-capacitance of the coil resulted in a sub-optimal design. Further work will be required to find a design that properly balances both inductance, and thus mutual inductance to the reader coil, with coil resistance and capacitance. Although the present work focused on 13.56 MHz, going to higher operating frequencies presently appear advantageous. For example, of the industrial, scientific and medical (ISM) bands currently available in the European Union (EU), the 27 MHz, 40.7 MHz, or 169.4 MHz appear especially suitable due to the high permissible power levels. These bands require duty cycle limitations of 0.1 % to 1 %, but this does not need to be a limitation in condition monitoring applications where measurement durations in the millisecond range and repetition rates on time-scale on the order of seconds can be sufficient.

6 Conclusion

We propose a concept of using wireless, direct-contact sensors with on-chip coils to accurately monitor the temperature of power semiconductors while providing galvanic isolation from them. A prototype chip with on-chip coil was manufactured as an initial step to assess the feasibility of this concept. Said chip demonstrate that attention need to be paid so that the coil capacitance, $C_{L_{\text{chip}}}$, does not become too large for the coil to be effective at high frequencies.

Earlier work that support the feasibility of this concept include [6] which have demonstrated power transfer efficiencies of around 1 % for on-chip coils. The coil of that work could be used with the sub-µW sensor demonstrated in [8] to realise the proposed monitoring scheme.

Acknowledgement

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Paper C

High-Temperature Characterisation of Leakage Current Compensated, Low-Power, Bandgap Temperature Sensors

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High-Temperature Characterisation of Leakage Current Compensated, Low-Power, Bandgap Temperature Sensors

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Abstract

This paper analyses leakage current compensation techniques for low-power, bandgap temperature sensors. Experiments are conducted for circuits that compensate for collector-substrate, collector-base, body-drain and source-body leakage currents in a Brokaw bandgap sensor.

The sensors are characterised and their failure modes are analysed at temperatures from 60 to 230 °C. It is found that the most appropriate compensation circuit depends on the accuracy requirements of the application and on whether a stable reference voltage is required by other parts of the circuit.

Experiments show that the power consumption is dominated by leakage current at high temperatures. One type of sensor was seen to consume 260 nW at 60 °C, 2.1 µW at 200 °C and 14 µW at 230 °C.

This work is motivated by the need to accurately monitor the temperature of power semiconductors in order to predict emerging faults in power semiconductor modules, a task for which cheap, single-chip, low-power, high-temperature, wireless bandgap temperature sensors are appropriate.

1 Introduction

High-temperature sensors are used in power electronic equipment to monitor the temperature of power semiconductors [1], and their use in this area is the main motivation behind this work. The ageing of the solder interface between power semiconductor and cooling baseplate causes an increase in operating temperature of the device over time and can eventually result in the device's destruction [2]. If a temperature rise can be detected before a device fault occurs, preventive maintenance can be performed, and catastrophic failure can be avoided.

Systems that measure the temperature of power semiconductors by using direct-contact sensors are not known by the authors to exist, but would provide advantages in terms of accuracy and portability between modules [3]. This work aims to enable the manufacturing of such a system by demonstrating a low-power integrated circuit (IC) temperature sensor that is able to operate up to at least 230 °C.

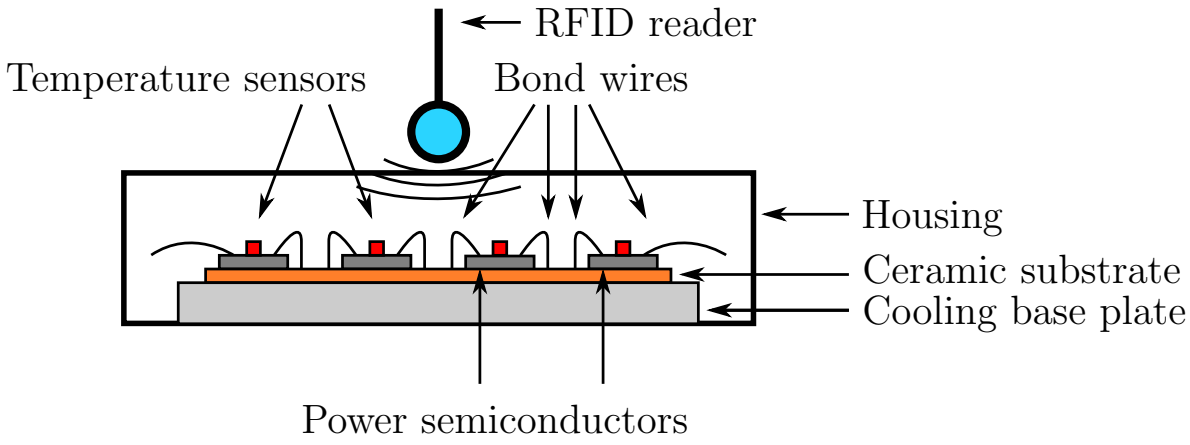


Figure 1: Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by a nearby RFID reader [4].

Low-power, high-temperature sensors can be used in conjunction with on-chip coils for power transfer to monitor the temperature of power semiconductors [4]. The concept is illustrated in Figure 1. Here, the temperature sensors are glued in direct contact with the power semiconductors to provide accurate measurements while being galvanically isolated from the main measurement system, as communication and power supply are implemented wirelessly through radio-frequency identification (RFID) technology.

One challenge in designing low-power, high-temperature bandgap temperature sensors is the exponential increase in leakage current with increasing temperature [3]. These leakage currents arise in reverse-biased p-n junctions [5]. Unless compensated for, this effect will set the upper operating temperature limit of a sensor.

This paper presents high-temperature characterisations of low-power temperature sensors by providing and analysing measured data of manufactured ICs in a 0.18 µm p-substrate CMOS process with vertical bipolar junction transistors (BJTs). The sensors are Brokaw bandgap temperature sensors with collector-substrate (CS) leakage current compensation from [6] for bipolar transistors. We also include circuitry for collector-base (CB) leakage current compensation as well as for body-drain (BD) and source-body (SB) leakage current compensation for metal-oxide semiconductor field effect transistors (MOSFETs). In these circuits, the NMOS and PMOS bodies are p-wells and n-wells connected to ground and supply voltage, respectively. Experiments are performed for temperatures up to 230 °C to characterise circuits with no leakage current compensation circuitry, with the compensation circuit found in [6] (previously characterised up to 175 °C) and with said compensation circuit plus the compensation circuit demonstrated in [3], which has previously only been characterised through simulation up to 175 °C.

The experiments show that the use of CB/BD/SB leakage current compensation circuits enable operation up to at least 230 °C. They further show that many of the sensors that do not use this type of compensation circuit fail at temperatures around 200 to 210 °C.

In Section 2, we present a survey of previous work on leakage current compensation techniques for bandgap circuits as well as the theory behind the sensor presented in this work. In Section 3, the experimental set-up is described, with the experimental results presented in Section 4. Section 5 presents a discussion of the results and compares them to the results of other works. Conclusions are presented in Section 6.

2 Low-Power Bandgap Temperature Sensors

The Brokaw bandgap reference [7] is commonly used to measure temperatures. One implementation is depicted in Figure 2. The basic idea is that the base-emitter (BE) voltage, V_{BE}, of a BJT has a negative temperature coefficient, whereas the difference in voltage between a larger and smaller BJT, ΔV_{BE}, has a positive temperature coefficient and is thus proportional to absolute temperature (PTAT). V_{BE} is given in [8] as

$$V_{\mathrm{BE}} = V_{\mathrm{G0}} - c_{\mathrm{T}} T + V_{\mathrm{NL}}(T). \tag{1}$$

Here, $V_{\mathrm{G0}} \approx 1.2\,\mathrm{V}$ is the extrapolated bandgap voltage at 0 K, c_{T} is a constant temperature coefficient, T is the temperature, and $V_{\mathrm{NL}}(T)$ represents temperature-dependent, non-linear terms. In this work, we ignore $V_{\mathrm{NL}}(T)$ because it is insignificant considering our desired accuracy and substantially smaller than the errors introduced due to leakage at high temperatures.

By summing and scaling ΔV_{BE} and V_{BE}, two new voltages are generated; one voltage that is constant over temperature, V_{REF}, and one that is PTAT, V_{PTAT}. The ratio of these voltages, $V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$, can be used in conjunction with an analogue-to-digital converter (ADC) to obtain temperature measurements.

2.1 Operation of the Brokaw Bandgap Reference

Ignoring the effects of Q_3 for now, the circuit of Figure 2 operates by having the current mirror M_1-M_2 force equal collector currents I_{C1} and I_{C2} through Q_1 and Q_2 using the common source transistor M_3 to feedback an error signal into the bases of Q_1 and Q_2.

Because Q_1 and Q_2 differ in size and carry equal collector currents, they are biased at different current densities, and thus, a voltage ΔV_{BE} develops across their emitters, that is, over R_1. Because ΔV_{BE} is PTAT, the current through R_1, I_{E2}, will be PTAT. Assuming equal emitter currents, $I_{\mathrm{E1}} = I_{\mathrm{E2}} = I_{\mathrm{E}}$, the current through R_2 ($2I_{\mathrm{E}}$) will also be PTAT, and therefore V_{PTAT} will be PTAT. The voltage V_{REF} will be the sum of V_{PTAT} and the base-emitter voltage of Q_1, V_{BE1}. Thus, scaling the ratio of R_2/R_1 appropriately makes V_{REF} independent of temperature and equal to V_{G0} because the first-order temperature-dependent terms are cancelled.

An expression for V_{PTAT} is given in [7] as

$$V_{\mathrm{PTAT}} = 2\frac{R_2}{R_1}\frac{kT}{q}\ln\frac{J_{\mathrm{C1}}}{J_{\mathrm{C2}}}, \tag{2}$$

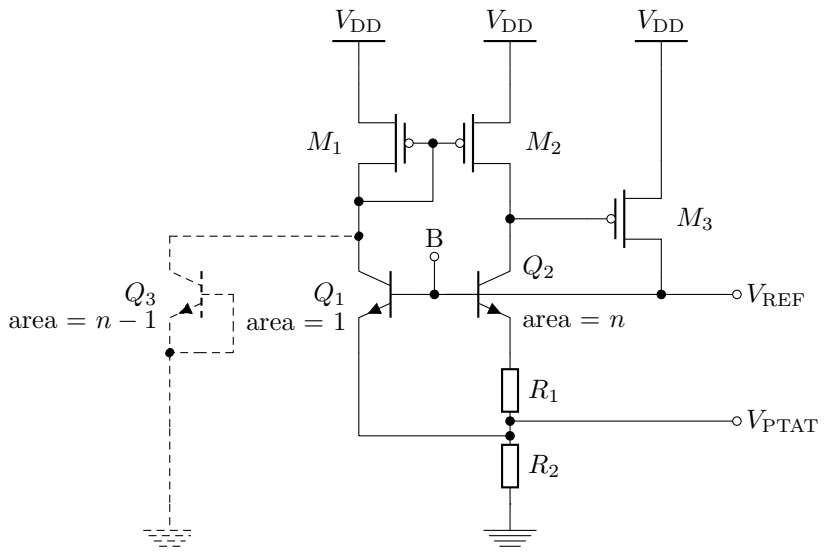


Figure 2: Brokaw bandgap reference circuit as implemented in [6]. For simplicity, the start-up circuit is shown sepearately in Figure 3 and is connected to this circuit through their common node B.

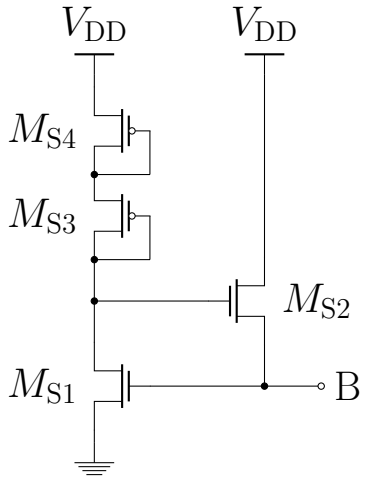


Figure 3: Start-up circuit for the Brokaw bandgap circuit of Figure 2. This circuit is connected to the bandgap circuit through their common node B.

where k is Boltzmann's constant, T is the temperature and J_{C1} and J_{C2} are the respective collector current densities of Q_1 and Q_2. If $I_{C1} = I_{C2}$, we can write

$$V_{PTAT} = 2\frac{R_2}{R_1}\frac{kT}{q}\ln\left(n\frac{I_{C1}}{I_{C2}}\right), \tag{3}$$

where n is the area ratio between transistors Q_2 and Q_1.

To avoid the operating point at which no current flows through Q_1 and Q_2, a start-up circuit must be introduced. This circuit is shown in Figure 3 and is connected to the circuit of Figure 2 through their common node B. It operates by having the pull-up network M_{S3}-M_{S4} turn M_{S2} on unless there is a voltage V_{REF} at node B to turn M_{S1} on, which then in turn drives M_{S2} off. This arrangement enforces a non-zero voltage, V_{REF} at node B.

2.2 Effects of Collector-Substrate Leakage Current in Bandgap Circuits

Leakage current poses a challenge in high-temperature IC design [5]. Figure 4 shows an extended version of the schematic in Figure 2, where major sources of leakage current due to reverse-biased p-n junctions are shown and indicated as current sources. In this figure, CS leakage occurs in Q_1, Q_2 and Q_3. Because leakage current in reverse-biased p-n junctions increases exponentially with increasing temperature [9], at high temperatures, the leakage currents of a low-power bandgap temperature sensor become significant as their magnitudes become comparable to that of the sensor's quiescent current. One aspect of how leakage current adversely affects bandgap circuits has been studied by Radoiaş *et al* [6, 10]. They found that, at high temperatures, CS leakage in the main bipolar pair causes the collector currents I_{C1} and I_{C2} to become mismatched due to differing sizes of the respective transistors.

The source-drain currents of M_1 and M_2 are the sum of their respective associated collector currents, I_{C1} and I_{C2}, and leakage currents, I_{CS1} and I_{CS2}, being drawn from the collectors of Q_1 and Q_2. Because Q_2 is larger than Q_1, $I_{CS2} > I_{CS1}$. The current mirror M_1-M_2 and the feedback loop through M_3 will keep $I_{C1} + I_{CS1} = I_{C2} + I_{CS2}$, by increasing the drain current of M_3, I_{D3}, supplied to the bases of Q_1 and Q_2. As the BE junction of Q_1 has a lower impedance than that of Q_2, I_{C1} will increase more than I_{C2}. Thus, taking leakage currents into account, the ratio I_{C1}/I_{C2} increases.

It can be seen from Eq. (3) that V_{PTAT} will increase from an increase in collector current ratio, I_{C1}/I_{C2}. This increase will also be seen in V_{REF} because V_{REF} is the sum of V_{PTAT} and V_{BE1}. Thus, at high temperatures, V_{PTAT}/V_{REF} increases beyond the level predicted if leakage current is not considered.

When the temperature, and hence CS leakage currents, become large enough, the collector voltages of Q_1 and Q_2 decrease and eventually the CB junctions of Q_1 and Q_2 become forward-biased. This causes a part of I_{D3} to go through the CB junctions of Q_1 and Q_2, reducing the current through their BE junctions. Thus, I_{C1} and I_{C2} are reduced, effectively reducing V_{PTAT} and V_{REF}. At sufficiently high temperatures, this

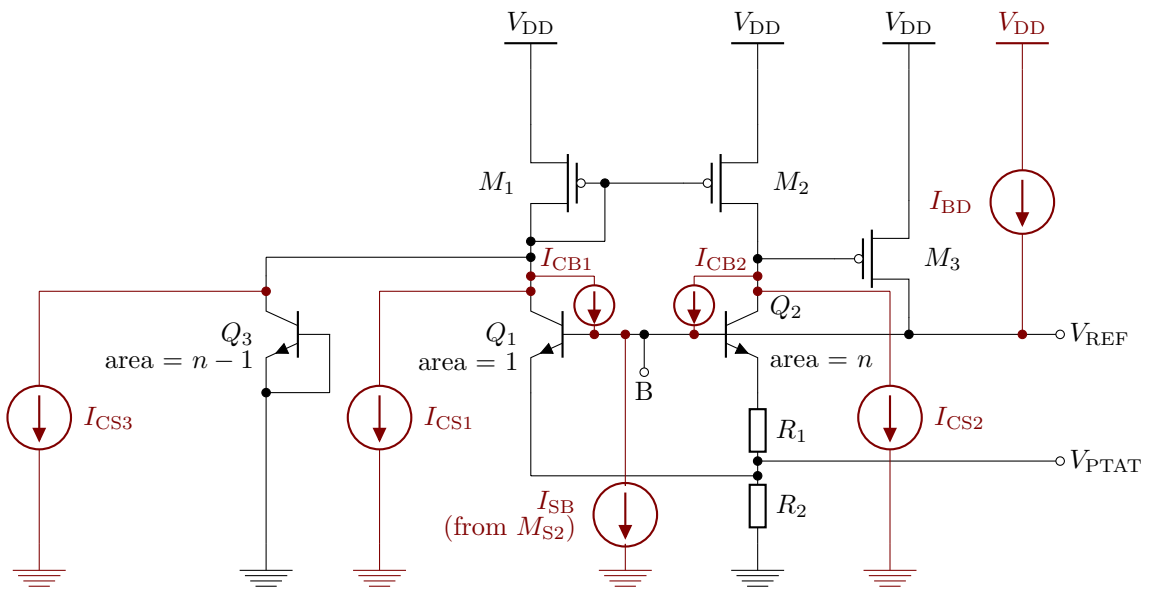


Figure 4: Brokaw bandgap circuit with leakage current caused by reverse-biased p-n junctions represented as current sources. The subscripts CS, CB, BD and SB indicate CS, CB, BD and SB leakage current, respectively.

effect prevents the circuit from operating as a bandgap reference, thus disabling its ability to function as a temperature sensor.

Radoiaş *et al* compensated for unequal CS leakage by introducing another transistor in cut-off mode with a size equal to the difference in size between the main bipolar pair, Q_1 and Q_2 [6]. This new transistor is Q_3 in Figure 2. The sole purpose of this transistor is to ensure that CS leakage currents in both half circuits are matched, therein keeping collector currents equal even at high temperatures and thus compensating for the non-linearities arising from CS leakage.

Note that Radoiaş *et al* connected the emitter and base of Q_3 to V_{PTAT} [6]. In contrast, in this work, we connect it to ground to avoid introducing non-linearities in V_{PTAT} (and subsequently in V_{REF}) caused by the CB leakage of Q_3.

2.3 Effects of Collector-Base, Body-Drain and Source-Body Leakage Current in Bandgap Circuits

Excess current introduced in the bases of the bipolar pair, node B in Figure 2, may adversely affect circuit operation, especially for low-power circuits [3]. Such an excess current arises at high temperatures due to CB, BD or SB leakage introduced by reverse-biased p-n junctions in Q_1, Q_2, M_3 and M_{S2}, see Figure 3 and Figure 4. In these figures, CB leakage occurs in Q_1, Q_2, and Q_3; BD leakage occurs in M_3, while SB leakage occurs in M_{S2}. Note that M_{S2} is leaking current out of node B, while the other leakages are leaking current into node B. However, summing all leakages from/to node B results in a net outflow of current from the node because the leaking junction area of the bipolar

transistors are significantly bigger than that of M_{S2}.

Because Q_1 is biased at a higher current density than is Q_2 and has no series resistor, the majority of excess current injected in node B will take the path through the BE junction of Q_1, be amplified by Q_1 and mirrored by the current mirror M_1-M_2. The gate voltage of M_3 will increase, whereby the current from M_3 supplied to node B will be reduced, counteracting the initially introduced current. However, if the loop gain of the M_1-M_2-M_3 feedback loop is low, non-negligible current imbalance between Q_1 and Q_2 will remain. Such an imbalance introduces non-linearities with respect to temperature in V_{REF} and V_{PTAT}. Because the CB junction of Q_3 is biased at a higher reverse voltage than are Q_1 and Q_2, the magnitude of its CB leakage current is slightly higher than that of Q_1 and Q_2. Thus, M_3 will subtract more current than are added in the form of CB/BD/SB leakage. At sufficiently high temperatures, M_3 will be turned completely off, whereas V_{REF} and V_{PTAT} will only be driven by leakage current, thus dropping to very low voltages.

Because CB/BD/SB leakage limits the high temperature range in which a bandgap sensor can operate, it is desirable to compensate for such leakage. Such compensation can be realised by adding artificial leakage sources in the form of transistors in cut-off with dimensions identical to that of the leaking transistors. This leakage can then be mirrored so that equal amounts of leakage is leaking into a node as is leaking out of it. Mizuno *et al* demonstrated such a compensation circuit in [11]. Because the direction of net leakage current in the Mizuno circuit (towards ground) is different from that in this work (towards supply), a modified circuit was presented in our previous work [3] and further extended in this work to compensate for one additional leaking transistor, M_{S2}. This circuit is presented in Figure 5. Here, sources of artificial leakage are generated by Q'_1, Q''_1, Q'_2, Q''_2, M'_3 and M'_{S2} operating in cut-off, while the current mirror consists of M_{C1}, M_{C2}, M_{C3}, M_{C4} and M_{C5}. See [11] for details of how this circuit operates. A discussion of failure modes for the circuits of Figure 4 and Figure 5 is presented in Section 4.1.

2.4 Matching of Leakage Currents

The success of leakage current compensation techniques are highly dependent on the matching that can be achieved between the compensated and the compensating device. In their work, Mizuno *et al* have demonstrated matching of leakage currents with an error of 5 % [11]. This increased the temperature operating range by 20 °C compared to using a simple current mirror as compensation circuit, by 40 °C compared to using a diode directly and by 60 °C compared to not using any leakage current compensation at all.

Because we use the same underlying compensation technique in this work for CB/BD/SB leakage current compensation, we expect a similar level of matching. Thus, we also expect the failure mechanisms involving by CB/BD/SB leakage to be shifted up in temperature by approximately 60 °C.

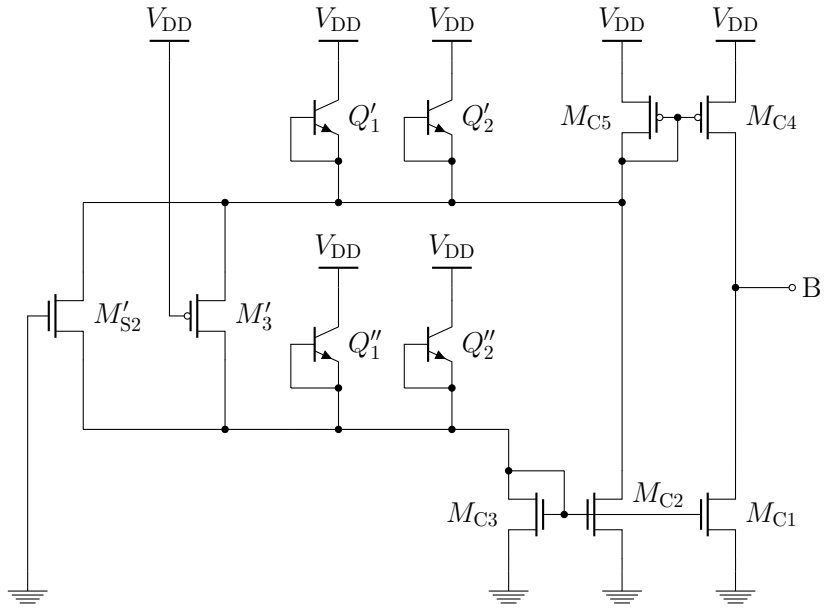


Figure 5: Leakage current compensation circuit connected to the Brokaw bandgap circuit of Figure 2. The prim/bis notation denotes devices with identical dimensions as similarly named devices from the Brokaw bandgap circuit depicted in Figure 2. M_{C1}, M_{C2}, M_{C3}, M_{C4} and M_{C5}, all have a width of $2\,\mu m$ *and a length of* $360\,nm$. *This circuit has been designed for a nominal supply voltage of* $V_{DD} = 2.0\,V$. *The only currents flowing in the circuit are leakage current and compensation current (mirrored leakage current). The circuit is based on the work of Mizuno et al [11].*

2.5 Power Consumption of Low-Power, High-Temperature Bandgap Sensors

The power consumption, P, of a Brokaw bandgap reference with the two leakage current compensation circuits described earlier in this section consists of two temperature-dependent components; a linear part, due to bias current, and an exponential part, due to leakage current [3]. The power consumption can be written as

$$P = c_1 T + c_2 e^{b_2 T}, \tag{4}$$

where T is the temperature and c_1, c_2 and b_2 are linear and exponential temperature coefficients.

At low temperatures, the magnitudes of leakage currents are small and the linear part will dominate. At higher temperatures, the exponential part becomes significant and rapidly becomes the dominant term in the expression for the power consumption. Thus, there is a limit below which a reduction in bias current is not effective for reducing the power consumption at high temperatures where the exponential term is dominant.

3 Experiments

To assess the contribution of each compensation technique presented in Section 2, measurements were performed on three types of bandgap sensors:

- Type 0: With no leakage current compensation; that is, the circuit of Figure 2 excluding Q_3.
- Type R: With the leakage current compensation circuit of Radioaş *et al* [6]; that is, the circuit of Figure 2 including Q_3.
- Type RN: With the leakage current compensation circuit of Radioaş *et al* [6] and the leakage current compensation circuit of Nilsson *et al* [3]; that is, the circuit of Figure 2 including Q_3 with the circuit of Figure 5 connected to it (node B to node B).

Because of the high operating temperatures and relatively high output impedance of V_{REF} and V_{PTAT}, bootstrapped guard rings [12] were implemented on the printed circuit board (PCB) where the device under test was bonded, and polytetrafluoroethylene-insulated (PTFE) wires were used for connecting this board to the remainder of the measurement set-up. The guard rings were implemented because surface leakage currents in the PCB were observed at high temperatures. Driving a guard ring to the same potential as that of the trace which it surrounds minimises this leakage. For each measurement the temperature was required to remain within $\pm 1\,^{\circ}\mathrm{C}$ (as measured using a Pt100 resistance thermometer) for 90 s, after which 50 measurements were taken. Because of problems with tuning the oven temperature regulator at high temperatures, several devices were damaged by epoxy leaking from the PCB, thus limiting the number of samples that could be fully characterised.

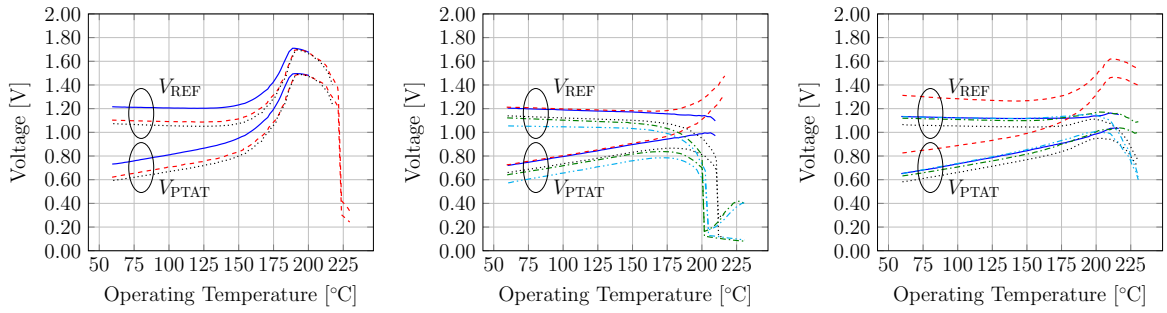
4 Measurement Results

A batch of $2.25\,\mathrm{mm}^2$ chips containing Type 0, Type R and Type RN circuits were manufactured in a 0.18 µm CMOS process with vertical npn BJTs. The dimensions used for the transistors are specified in Table 1. Temperature sweeps were performed on each type of circuit, and data for all the sweeps of V_{REF} and V_{PTAT} for the different types of circuits is presented in Figure 6. Due to the difficulties encountered during the characterisations (as described in Section 3), we were only able to successfully complete temperature sweeps on 3 different Type 0 circuits, 5 different Type R circuits and 5 different Type RN circuits. Due to the limited sample size, we do not present standard deviations for the measured data.

Different properties of the different types of compensation circuits are analysed in the remainder of this section. Unless otherwise noted, the presented data is for a supply voltage V_{DD} of 2.0 V.

Table 1: Dimensions of transistors from the circuits of Figure 2, Figure 3 and Figure 5 for a 0.18 µm *design.*

Device		
MOSFETs	*width* [nm]	*length* [nm]
M_1, M_2	2000	360
M_3	2000	720
M_{S1}, M_{S2}	2000	360
M_{S3}, M_{S4}	220	20 000
M_{C1}, M_{C2}, M_{C3}, M_{C4}, M_{C5}	2000	3600
BJTs	*emitter area* [µm^2]	
Q_1	6.8 (1 device)	
Q_2	40.8 (6 devices)	
Q_3	34.0 (5 devices)	



(a) Type 0 (b) Type R (c) Type RN

Figure 6: Measurement results of V_{REF} and V_{PTAT} as functions of temperature for different types of leakage current compensation circuits. Each plot contains data from multiple temperature sweeps from different chips. Identical line styles in a plot indicate voltages from the same chip.

4.1 Failure Modes

From Figure 6a it can be seen that the failure mode for Type 0 circuits follows the theory presented in Section 2.2. At moderately high temperatures both V_{REF} and V_{PTAT} increase, whereas at higher temperatures, they rapidly decrease to very low values.

For Type R circuits, it can be seen from Figure 6b that for most circuits V_{REF} and V_{PTAT} become very low voltages at high temperatures. This is in agreement with the theory presented in Section 2.3. When M_3 is turned off, V_{REF} is reduced to the point at which it triggers the start-up circuit of Figure 3. Because the start-up circuit is triggered at the threshold voltage of M_{S1}, V_{REF} attains the value of said threshold voltage and because threshold voltage decreases with temperature [5], V_{REF} also decreases with temperature.

As V_{REF} decreases in Type R circuits, it can be seen from Figure 6b that V_{PTAT} starts to increase beyond V_{REF}. Because V_{PTAT} is larger than V_{REF} it can no longer be driven by V_{REF}. Thus, the current through R_2 must come from another place than node B. Looking at the circuit of Figure 2, it can be seen that the current can only come from one or both of the bipolar transistors, Q_1 and Q_2. One feasible explanation for this behaviour is collector-emitter (CE) leakage current from pipe formation or surface inversion in the base [13]. Although surface inversion in bipolar devices is uncommon in modern processes, a reduced threshold voltage due to the unusually high operating temperature of the devices under test might trigger the phenomenon. Another source of CE leakage could be minority holes from the CB junction diffusing over to the BE junction instead of exiting through the base. This effect would be more prominent when the BE junction is reverse-biased, which it is at this operating point, because a reverse biased BE junction would decrease the effective base width. For the two temperature sweeps on Type R circuits where this effect could be observed, around 450 nA was seen to run through R_2 at 225 °C.

One exception to the behaviour discussed above is the red, dashed line of Figure 6b. Here, V_{REF} and V_{PTAT} increase instead. One explanation for this deviation from the theory could be that for that particular circuit, a mismatch in the bipolar transistors occurred so that the left half-circuit of Figure 2 (Q_1 and Q_3) generates significantly less CS leakage current than the right half-circuit (Q_2). The failure mode of this circuit then becomes similar to that of Type 0 circuits except that it occurs at higher temperatures because the CS leakage for each half-circuit is still better matched compared to Type 0 circuits.

From Figure 6c it can be seen that for Type RN circuits similar non-linearities as for the Type R circuit are present, although at higher temperatures compared to the Type R circuits. No rapid voltage reductions as seen in Type R circuits was seen in Type RN circuits at the examined temperatures. However, due to mismatches in compensated leakage currents resulting from process mismatches and/or the limitations of the compensation circuits used, it is likely that the Type RN circuits would fail in a manner similar to the other circuits, but that the failures occur at temperatures higher than the temperature range of the experiments performed in this work. As concluded in Section 2.4, if similar matching to that of [11] was achieved, this failure mode should occur for Type RN circuits at a temperature approximately 60 °C higher than the temperature at which this happens for Type R circuits. However, the temperature sweeps performed in this work do not examine such high temperatures. Thus, this hypothesis has yet to be confirmed.

4.2 Linearity, Accuracy and Temperature Range

For Type 0 circuits (Figure 6a) significant non-linearities are introduced in V_{REF} and V_{PTAT} at temperatures as low as 150 °C. For Type R and Type RN compensations, it can be seen from Figure 6b and Figure 6c that the same magnitude of non-linearities do not occur until above 175 °C.

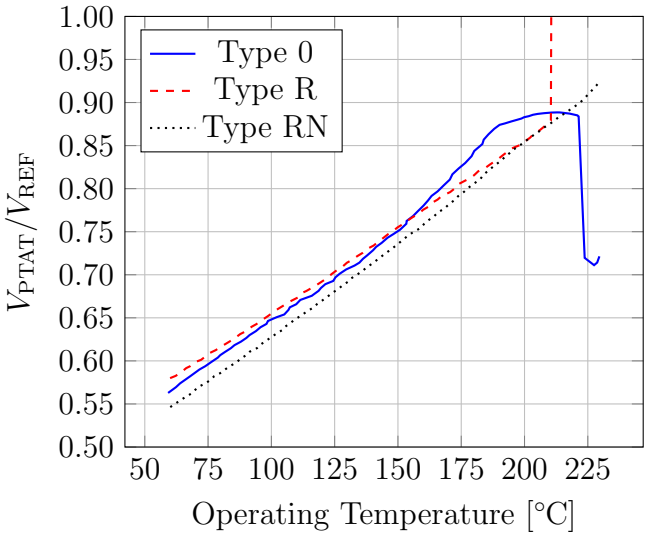


Figure 7: Measurement results of V_{PTAT}/V_{REF} as functions of temperature for different types of leakage current compensation circuits for a Brokaw bandgap circuit. The Type 0 curve is derived from the red dashed curve from Figure 6a, and the Type R and RN curves are derived from the black dotted curves of Figure 6b and Figure 6c, respectively.

Figure 7 shows a $V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$ ratio for different types of compensation circuit based on data of selected curves from Figure 6. The curves were not chosen to quantify performance, but rather to illustrate the characteristic behaviour of each of the different types of compensation circuit. The selected graphs are from sweeps from which the highest temperature ranges were obtained. For the Type 0 circuit, the curve is highly non-linear and experiences a rapid decrease at 220 °C, where both V_{REF} and V_{PTAT} are reduced rapidly. The Type R circuit achieves good linearity up to 210 °C, followed by a rapid increase in $V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$ where both V_{REF} and V_{PTAT} fall off sharply. The Type RN circuit, on the other hand, presents good linearity over the entire 60 to 230 °C temperature range.

The data of the $V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$ ratio was used to assess the linearity of the different types of compensation circuits and to relate the linearity to how it affects the temperature range for a given accuracy. Table 2 presents the best-case, median and worst-case ranges over which a least-squares fit to measured data in the 60 to 90 °C temperature range produced a maximum deviation of 3, 5 and 10 °C. We denote this deviation as the accuracy of the circuit. Examining the median upper temperature limits, it can be seen that the Type 0 circuit has the lowest upper temperature limit for all values of accuracy. For the 3 °C and 5 °C accuracy requirements, the Type R circuit achieves the highest upper temperature limit, and the Type RN circuit achieves the highest upper temperature limit for an accuracy of 10 °C.

To further assess the accuracy of the circuits, histograms presenting the amount of chips which achieved a given accuracy at different temperatures are presented in Figure 8. It can be seen from Figure 8a that at 195 °C, all of the 5 measured Type R circuits achieve

Table 2: Upper temperature limits for different types of leakage current compensation circuits for different values of accuracy. For each type of compensation and for a certain accuracy, the best, median and worst chips in terms of highest upper limits are shown in the following format: "<best-case> / <median> / <worst-case>". The maximum V_{REF} variation over the range where the accuracy is not exceeded is also shown. An identical position or colour for a given accuracy indicates data from the same chip.

Accuracy [°C]	**Upper Temperature Limit** [°C]		
	Type 0	*Type R*	*Type RN*
10	171/162/161	216/210/200	228/216/181
5	156/155/153	208/200/184	202/182/158
3	150/147/144	200/170/162	182/168/147
	Maximum V_{REF} Variation [mV]		
	Type 0	*Type R*	*Type RN*
10	140/74/65	258/303/283	257/46/53
5	42/30/28	270/283/36	22/22/48
3	24/22/16	283/36/32	17/16/48

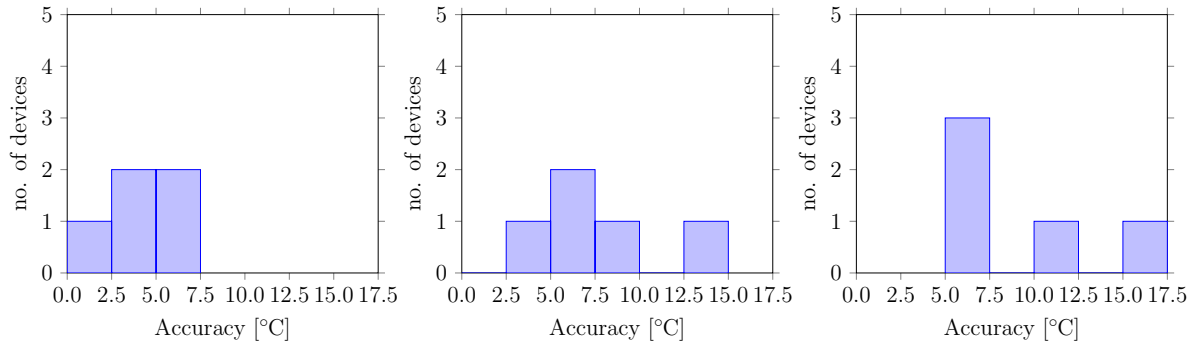
an accuracy better than 7.5 °C. This is in contrast to the Type RN circuits for which the accuracies are generally worse and varies more. Figure 8b shows that 4 of the 5 measured Type RN circuits achieve an accuracy between 2.5 and 10.0 °C whereas 3 of those stay below 7.5 °C. The histograms are shown at 195 °C because several of the Type R circuits experienced malfunction at around 200 °C. Looking at a higher temperature of 216 °C, it can be seen from Figure 8c that the accuracy for Type RN devices is slightly reduced but still stays better than 7.5 °C for 3 of the 5 tested chips. Data of Type R devices for 216 °C is not presented because the Type R devices that were characterised up to that temperature experienced malfunction at 210 °C or lower.

4.3 Reference Voltage Stability

Table 2 also shows the maximum V_{REF} variation over the temperature range where the accuracy requirement is not exceeded. For the chips with median upper temperature limit, it can be seen that the Type RN circuit has a generally more stable V_{REF} over temperature than has the Type R circuit.

The obtained results were compared to the simulations of [3]. For Type RN circuits with an accuracy of 3 °C the median upper temperature limit is 168 °C for which V_{REF} varies by 16 mV. This result is in agreement with expected values based on simulation results from [3]. There, a Monte Carlo simulation showed a variation of V_{REF} of 9.4 mV over the 0 to 175 °C temperature range, with a standard deviation of 6.8 mV.

As can be seen from Figure 6a, the V_{REF} stability of the Type 0 circuit is generally



(a) Type R, 195 °C (b) Type RN, 195 °C (c) Type RN, 216 °C

Figure 8: Histograms of the accuracy for Type R and Type RN circuits for 195 *and* 216 °C*. Data for each plot is derived from 5 temperature sweeps of different chips for both Type R and Type RN circuits. Data for Type R circuits at* 216 °C *has been omitted because all Type R devices characterised at said temperature experienced malfunction at* 210 °C *or lower, as can be seen from Figure 6b.*

low. However, we do not compare it to the other types of circuits because its upper temperature limit is significantly lower than that of the other circuits.

4.4 Supply Voltage Requirements

When repeating the above experiments for a supply voltage $V_{\mathrm{DD}} = 2.5\,\mathrm{V}$, V_{REF} and V_{PTAT} were largely unaffected for most sweeps. However, for two out of thirteen measurements, a difference was seen at high temperatures. One possible explanation is that the hole mobility decreases with increasing temperature and a larger overdrive voltage over the M_1-M_2 mirror is required for a given current for the mirror to remain in saturation. In addition, leakage currents from the collectors of Q_1 and Q_2 must be resupplied by the current mirror, further increasing the required overdrive voltage. This phenomenon was seen for one of the Type 0 circuits, none of the Type R circuits and one of the Type RN circuits.

4.5 Power Consumption

A plot of the mean power consumption based on four temperature sweeps of the Type RN circuit is shown in Figure 9. In accordance with the theory presented in Section 2.5, the power consumption consists of a linear term and an exponential term. The exponential coefficient b_2 was obtained from the exponential part of the plotted data and found to be $0.064\,^{\circ}\mathrm{C}^{-1}$. This supports the theory that the exponential term is due to reverse leakage current, which approximately doubles for every 10 °C increase in temperature [14].

At 60 °C, the power consumption of the different chips ranged from 230 to 320 nW (mean 260 nW), which is a relative variation of 32 %. At 200 °C, the power consumption ranged from 1.5 to 2.8 µW (mean 2.1 µW), reaching the higher relative variation of 60 %,

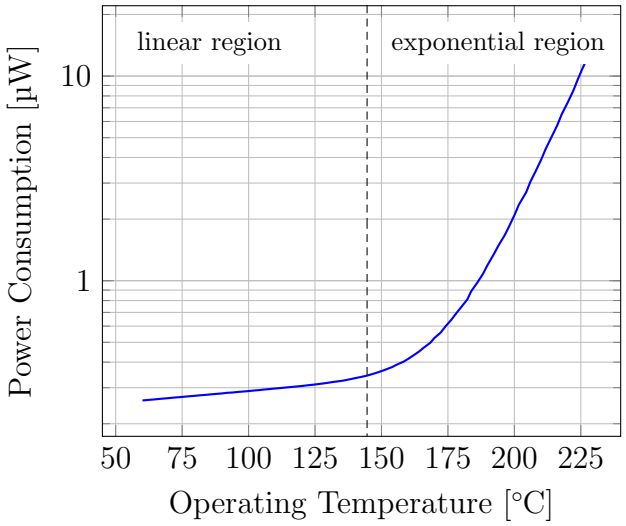


Figure 9: Mean power consumption of the Type RN circuit based on measured data from four temperature sweeps.

and at 230 °C, the power consumption ranged from 9.5 to 19 µW (mean 14 µW), reaching a relative variation of 67 %. This variation of power consumption between different regions of operation suggests that the power consumption generated by leakage current is more sensitive to process variation than is the power consumption generated by bias current.

5 Discussion

From the results presented in Section 4.2, it can be seen that two aspects play an important role when determining which compensation type to use when designing a low-power, high-temperature bandgap temperature sensor: how important it is to generate a stable reference voltage and how high of a measurement accuracy that is required.

5.1 Stable Reference Voltage

An advantage of using a bandgap circuit as a temperature sensor is that one of the generated output voltages is a relatively temperature-invariant reference voltage that can be used by other parts of the circuit that is not directly taking ratiometric temperature measurements. For example, an ADC may be needed to obtain digital samples of the measured voltages, or a voltage regulator in a mixed-signal design may need a stable voltage reference to operate properly. Thus, depending on the system specifications, because a Type RN circuit outperforms a Type R circuit in terms of V_{REF} stability, it may be preferable to use a Type RN circuit even though its temperature range is generally lower for an accuracy of 5 °C or better.

Table 3: Comparison of the performance of different temperature sensors. This work is included three times to demonstrate how the performance parameters change with changing requirements on accuracy. Power consumption is taken as the highest value over the entire temperature range. This table is based on the comparison table found in [15].

Parameter	**This Work[1]**	**This Work[2]**	**This Work[3]**	**[15]**	**[16]**	**[17]**
Sensing Element	bandgap	bandgap	bandgap	bandgap	bandgap	PIN diode
SOI	no	no	no	yes	yes	yes
Calibration Points	2	2	2	1	1	2
Process Technology Node [µm]	0.18	0.18	0.18	1.0	0.16	*not available*
Power Consumption (including ADC) [µW]	*not available*	*not available*	*not available*	90	40	150
Power Consumption (excluding ADC) [µW]	5.7	2.1	0.53	45	22	12
Accuracy [°C]	10	5	3	1.6	0.4	3
Temperature Range [°C]	60 - 216	60 - 200	60 - 170	40 - 170	−55 - 200	25 - 250

[1]The Type RN circuit corresponding to the measurements of the blue solid line of Figure 6c.

[2]The Type R circuit corresponding to the measurements of the green dashed-dotted line of Figure 6b.

[3]The Type R circuit corresponding to the measurements of the red dashed line of Figure 6b.

5.2 Accuracy and Temperature Range

If an accuracy better than 5 °C is required, it has been demonstrated that the Type R circuit provides the highest operating temperature range. However, if the accuracy requirement is relaxed to 10 °C, which may be acceptable for a condition monitoring system, the Type RN circuit achieves the higher range.

Although most samples of the Type R circuit outperforms the Type RN circuit in terms of temperature range at better accuracies than 5 °C, some Type R chips were shown to suffer from rapid reductions in output voltage at a specific temperature where both V_{REF} and V_{PTAT} fall off sharply. If V_{REF} becomes small, voltage regulators and subsequently digital subsystems requiring a regulated voltage in order to operate will shut down, reducing the possibilities for the system to signal that there is a problem. This behaviour was not seen for any of the Type RN chips in the temperature range where the experiments were performed, that is, from 60 °C to 230 °C. Thus, it would appear that Type RN circuits could operate at a higher temperature range, although with lower accuracy, while keeping a digital subsystem operational.

Another aspect of the fact that no such malfunction was seen for Type RN circuits is that the accuracy can be significantly improved if the system is calibrated digitally, and the difference in accuracy between a Type R and Type RN compensation circuit can be minimised, and thus, the operating range for a certain amount of accuracy can be extended. For circuits suffering from this type of malfunction, such a calibration will not improve the accuracy after the rapid voltage reduction point because too severe non-linearities are introduced there.

5.3 Comparison to Other Work

Table 3 presents a comparison of the sensor in this work in terms of different requirements on accuracy with state-of-the-art low-power, high-temperature sensors. The sensors in this work have no integrated ADC, and thus no power consumption value for those positions. Future work includes investigating how to combine a power-efficient ADC with the circuits presented in this work.

The sensors from this work show a higher or equal upper temperature limit compared to all other sensors with a bandgap as the sensing element. However, this is achieved at the expense of accuracy. For the case of a sensor in this work with an accuracy of 5 °C, the same upper temperature limit is obtained as in [16], and the power consumption is smaller by a factor of 17. However, [16] achieves an accuracy as high as 0.4 °C.

The only non-bandgap sensor in this comparison, [17], achieves an upper temperature limit as high as 250 °C. This is significantly higher than the sensor of this work even if an accuracy of only 10 °C is accepted. However, this is achieved with the power consumption increased by a factor of 18 compared to the sensors of this work.

In contrast to the other sensors in this comparison, the sensors from this work were not manufactured in an silicon on insulator (SOI) process to achieve a high upper temperature limit. Because leakage currents are generally smaller in SOI processes, it is possible that the temperature range could be further extended and/or the power consumption could be

reduced using such a process.

6 Conclusion

Experiments show that Type R and Type RN circuits extend the temperature range compared to the Type 0 circuit by 20 to 50 °C. For an accuracy of 10 °C or more, the Type RN circuit achieves a higher upper temperature limit compared to the Type R circuit, and for an accuracy of 5 °C or less, the Type R circuit achieves the higher limit. Some of the examined Type R circuits were seen to experience a total circuit malfunction above a certain temperature where no temperature readings can be conducted. This phenomenon was not seen for any of the Type RN circuits over the entire temperature range from 60 to 230 °C.

At high temperatures, the power consumption of the temperature sensors was found to be highly dependent on leakage current. It was seen to increase exponentially with increasing temperature, setting a limit at which it is no longer effective to reduce the power consumption by reducing bias current.

The sensors presented in this work are suitable for use in the field of condition monitoring of power semiconductors. Their high upper temperature limit and low power consumption make direct-contact sensors suitable for wireless single-chip designs. A drawback to using these types of sensors is their low accuracy; however, the trade-off between high temperature operation and high accuracy may be acceptable depending on the system requirements. Furthermore, the accuracy may be improved by calibrating the sensors digitally.

Acknowledgement

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Paper D

Chip-Coil Design for Wireless Power Transfer in Power Semiconductor Modules

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Errata: Due to an error in the simulation model, values given for resonant freuency and power transfer efficiency are overestimated. See Paper F for more accurate simulations. A report of this error has been submitted to the publisher.

Chip-Coil Design for Wireless Power Transfer in Power Semiconductor Modules

Joakim Nilsson, Johan Borg and Jonny Johansson

Abstract

This paper presents electromagnetic simulations of a wireless power transfer system suitable for a monitoring system for detection of solder fatigue in power semiconductor modules. Power is provided wirelessly from a printed spiral coil on a printed circuit board to a silicon chip with an on-chip coil. We use and adapt a known gradient-ascent-based optimisation algorithm to obtain suitable coil geometries. For a frequency of 433 MHz, the simulations show an efficiency of -34.7 dB which we conclude is sufficient for the proposed monitoring system.

1 Introduction

Solder faults in power semiconductor modules constitute a significant amount, 34 % of total failures in power electronic equipment [1]. It is thus desirable to monitor these faults so that they can be predicted and preventive maintenance can be performed before a failure occurs in order to avoid secondary or catastrophic failures. One way of predicting emerging faults is by monitoring the temperature of the power semiconductors [2]. A rise in temperature is an indication of emerging solder fatigue; voids forming in the solder interface between power semiconductor and base plate within a power semiconductor module, see Figure 1 [3]. These voids reduce the cooling efficiency of the solder interface and may result in overheating and subsequent destruction of the power semiconductor device.

A wireless monitoring scheme for solder fatigue was proposed in [2] and is depicted in Figure 2. Here, a radio-frequency identification (RFID) reader in the form of one or multiple printed spiral coils (PSCs) on a printed circuit board (PCB) communicate with and provide power to low-power (in the order of 10 µW) temperature sensors with on-chip coils mounted on top of the power semiconductor devices. A wireless design has the advantage of providing galvanic isolation from the power semiconductors. Other advantages include that the system design becomes easily portable between power semiconductor modules, direct-contact of sensor with power semiconductor enables accurate measurements, and that no knowledge about the inner workings of the power semiconductor is required [2].

This paper presents the design methodology for, and the simulations of, a PSC coupled to an on-chip coil within a power semiconductor module. To design the coils with high power transfer efficiency and adequate output voltage, we used a slightly modified version of the algorithm presented by Zargham and Gulak in their work on coil design for

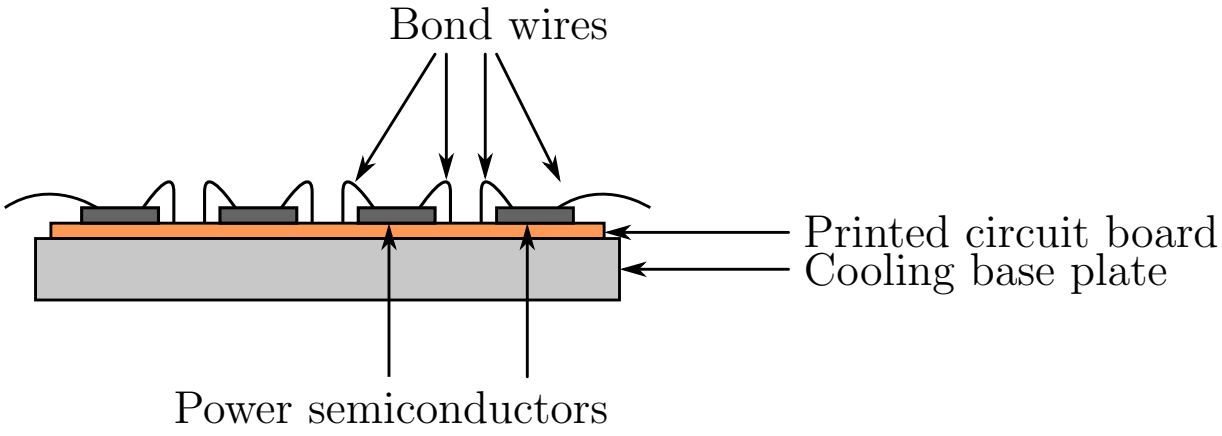

Figure 1: Schematic view of the cross-section of a wire-bond power semiconductor module.

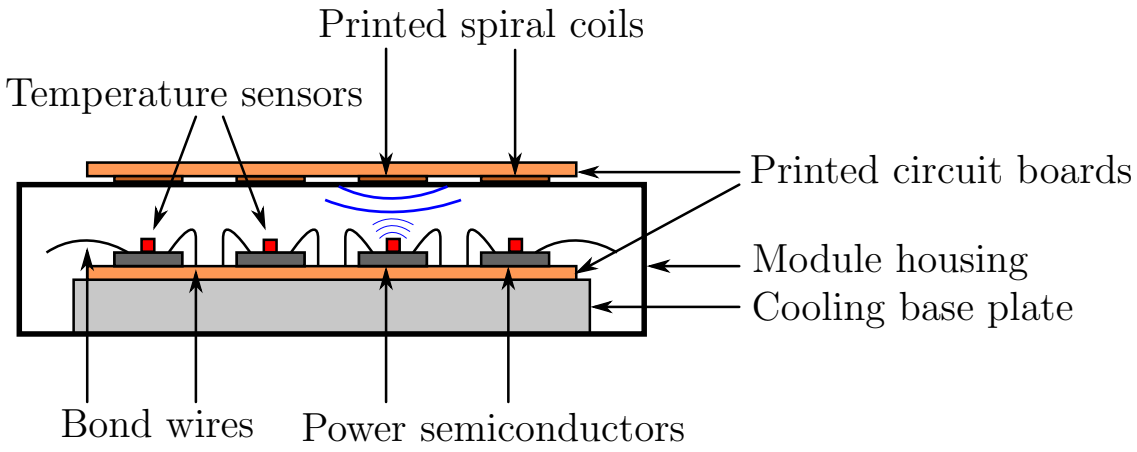

Figure 2: Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by printed spiral coils mounted outside of the module.

biomedical implants [4]. The power transfer efficiency and output voltage demonstrated show that this algorithm can be used not only for implantable on-chip coils, but also for coils in power semiconductor modules.

This paper is organised as follows. In Section 2 we present the geometry of the propsed monitoring system. In Section 3 we present the optimisation algorithm with the simulation results in Section 4. In Section 5 we provide a discussion and comparison with other work and finally we provide a conclusion in Section 6.

2 Power Semiconductor Module Geometry

A schematic view of the geometry of a wire-bond power semiconductor module and a complementary metal-oxide semiconductor (CMOS) silicon chip as well as the different types of internal materials is shown in Figure 3. Relevant parts of the monitoring system

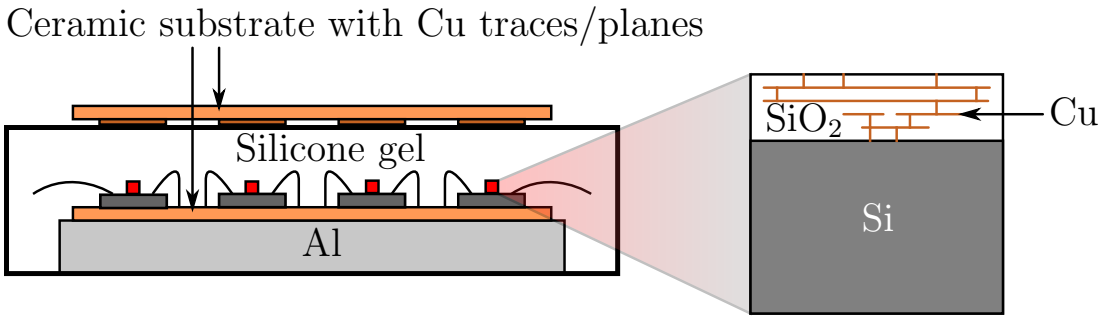

Figure 3: Materials in the proposed monitoring system.

proposed in the introduction are also shown. The module housing is filled with a silicone dielectric gel. A ceramic substrate with power semiconductors soldered on top of it is attached onto a cooling base plate located at the bottom of the module. For our proposed monitoring system, temperature sensors are glued on top of the power semiconductors. In this work, we present simulations of two coils, one PCB coil and one on-chip coil separated by 10 mm in a gel-filled power semiconductor module.

2.1 Chip Geometry

The bottom part of the temperature sensor chips consists of a lightly doped, p-type silicon substrate with low conductivity. The top part consists of a silicon oxide layer as well as copper traces. The process used in this work features 4 copper metal layers. Out of these four, the two top layers constitute the on-chip coil, shorted together with vias in the corners. Metal layer 2 (the second metal layer counting from the bottom) was not used at all for the coil and metal layer 1 was used as shielding from the conductive substrate. The shield consists of a chopped-up coil placed directly underneath the on-chip coil.

2.2 Material properties

Material properties for the materials used for the simulations of the proposed sensor system are presented in Table 1. For all materials except for the silicone gel, the values are well-known. The relative permittivity, ε_r for the silicone gel was obtained by a capacitance measurement of the gel used in a common power semiconductor module.

3 Coil Geometry Optimisation

To implement the monitoring system proposed in the introduction, an inductive link between the PCB coils located on the outside of the power semiconductor module and the on-chip coils of sufficient power transfer efficiency must be designed. In this paper, we demonstrate how we use an optimisation algorithm, originally presented by Zargham and Gulak [4], to achieve a sufficiently high power transfer efficiency for our proposed monitoring system.

Table 1: Material properties for the materials used in this work. Unit for conductivity corrected after publication.

Material	**Rel. permittivity** (ε_r)	**Conductivity** (σ) [MS/m]
Silicon substrate	11.7	*not available**
Silicon dioxide	3.9	∼0
Silicone gel	2.1	∼0
FR-4	4.4	∼0
Copper	1	59.6

*Value known and used for simulations, but can not be published due to non-disclosure agreement.

3.1 Simulation Model

A PSC is characterised by the following parameters: trace width, W; trace separation, S; coil outer dimension, d; and number of turns, N. An electromagnetic model for two coils separated by the media present in a power semiconductor module by a distance, D, was created. The electromagnetic simulator, FEKO [5], was used to evaluate the quality factors and power transfer efficiencies of these two coils. The model includes the media within the power semiconductor module, the materials and dimensions of a PCB as well as the materials and dimensions for a chip manufactured in a 0.35 µm CMOS process. To speed up simulation times, this model was simulated in 2.5D mode, where the dielectric materials presented in Table 1 were represented as infinite planes in the horizontal direction.

3.2 Algorithm

The algorithm used is similar to the one used in the work of Zargham and Gulak and for a detailed description we refer the reader to their work [4]. However, we present the psuedocode for our version of the algorithm in Table 2.

The main differences between our algorithm and that of Zargham and Gulak is how we use frequency in our simulation and what is included in the power transfer efficiency, η.

Frequency

Zargham and Gulak continuously swept a range of frequencies in each iteration of the gradient ascent algorithm [4]. However, for our application it would be beneficial if the frequency was selected to lie within a frequency band where higher levels of radiated power are permitted. By using one of these bands, and if a sufficiently high power transfer efficiency is achieved, the radiated power may fall below the allowed maximum value without the need for the system to be shielded.

For our simulations, the optimisation algorithm was run on a set of select frequencies;

Table 2: Power transfer effiiency optimisation algorithm for coil geometries

step 1: initialisation

$N_{\text{pcb}} := 2$

$W_{\text{pcb}} :=$ minimum allowed PCB width

$S_{\text{pcb}} :=$ minimum allowed PCB spacing

$d_{\text{pcb}} := D \cdot \sqrt{2\left(1+\sqrt{5}\right)}$

$N_{\text{chip}} := 2$

$W_{\text{chip}} :=$ minimum allowed chip width

$S_{\text{chip}} :=$ minimum allowed chip spacing

$d_{\text{chip}} :=$ chip die size

step 2: PCB coil quality factor optimisation

for $2 \leq N_{\text{pcb}} \leq 5$:
  gradient ascent algorithm:
    search: N_{pcb}, W_{pcb}, S_{pcb}
    maximise: Q
update: N_{pcb}, W_{pcb}, S_{pcb} for maximum Q

step 3: on-chip coil quality factor optimisation

for $2 \leq N_{\text{chip}} \leq 5$:
  gradient ascent algorithm:
    search: N_{chip}, W_{chip}, S_{chip}
    maximise: Q
update: N_{chip}, W_{chip}, S_{chip} for maximum Q

step 4: PCB-coil-based power transfer efficiency optimisation

for $2 \leq N_{\text{pcb}} \leq 5$:
  gradient ascent algorithm:
    search: N_{pcb}, W_{pcb}, S_{pcb}, d_{pcb}
    maximise: η
update: N_{pcb}, W_{pcb}, S_{pcb}, d_{pcb} for maximum η

step 5: on-chip-coil-based power transfer efficiency optimisation

for $2 \leq N_{\text{chip}} \leq 5$:
  gradient ascent algorithm:
    search: N_{chip}, W_{chip}, S_{chip}
    maximise: η
update: N_{chip}, W_{chip}, S_{chip} for maximum η

step 6: stop condition

if η improved since step 4:
  go to step 4
else:
  stop

namely 40.66 MHz, 169.4 MHz, 433.0 MHz and 868.0 MHz. The frequencies are chosen to lie within the industrial, scientific and medical (ISM) bands recommended by International Telecommunications Union (ITU) [6] and the frequency bands recommended by the Swedish Post and Telecom Authority (PTS) [7].

Power Transfer Efficiency

The other difference comes down to what is included in the power transfer efficiency, η. Zargham and Gulak optimised for a power transfer efficiency for a 2-port network with the assumption that the network is driving an optimal load [4]. Such a load can theoretically be realised using matching networks, but for on-chip coils and especially for light loads, large inductances would be required. Thus, the matching inductor may not be practical to manufacture on-chip with sufficiently high quality factors.

When evaluating the power transfer efficiency, we only include a single capacitor in the on-chip matching network. It has been estimated earlier that for a temperature monitoring system, 10 µW will be sufficient [8]. Therefore we assumed a 100 kΩ load for our simulations because such a load would consume 10 µW at a supply voltage of 1 V.

4 Simulation Results

The algorithm presented in Table 2 was run for the following frequencies: 40.66 MHz, 169.4 MHz, 433.0 MHz and 868.0 MHz for a coil separation, $D = 10$ mm. Out of those frequencies, the optimisation algorithm yields the best results for 433 MHz, so in this section the results of simulations for 433 MHz are presented. A 2.0×2.0 mm^2 integrated circuit (IC) design for a 0.35 µm process with the dimensions obtained from the simulations presented in this work has been submitted for fabrication.

For the on-chip coil, the simulation algorithm yields the highest power transfer efficiency for a trace width of 48 µm. However, the design rules the 0.35 µm used do not allow such wide traces, thus the trace width was adjusted to 35 µm with only a minor impact on power transfer efficiency. Furthermore, while the algorithm calculated a trace separation of 0.6 µm, theoretical calculations revealed that the major capacitance contribution comes from the coil and not from the on-chip capacitor for such a small trace separation. This may pose a problem to achieve the desired resonant frequency if the process parameters are not modelled accurately enough. Therefore, this value was adjusted to 6.0 µm and the value for the on-chip capacitor was recalculated. For the adjusted geometry, the on-chip capacitor, which is known to a greater accuracy compared to the coil capacitance, is the major contributor for capacitance. These adjustments reduced the power transfer efficiency by 0.5 dB. The final dimensions for both PCB and on-chip coil are presented in Table 3, while an image of the resulting chip coil is presented in Figure 4. Using those parameters for our simulations as well as an on-chip, parallel 1.20 pF capacitor yields a power transfer efficiency of −34.7 dB. The PCB coil's outer dimension of 25.4 mm makes it sufficiently small to fit on top of most power semiconductor modules.

Table 3: Coil geometries optimised for 433 MHz

Parameter		**PCB coil**	**On-chip coil**
Trace width,	W	3500 µm	35 µm
Trace seperation,	S	840 µm	6.0 µm
Outer dimension,	d	25.4 mm	2.0 mm
No. of turns,	N	2	5

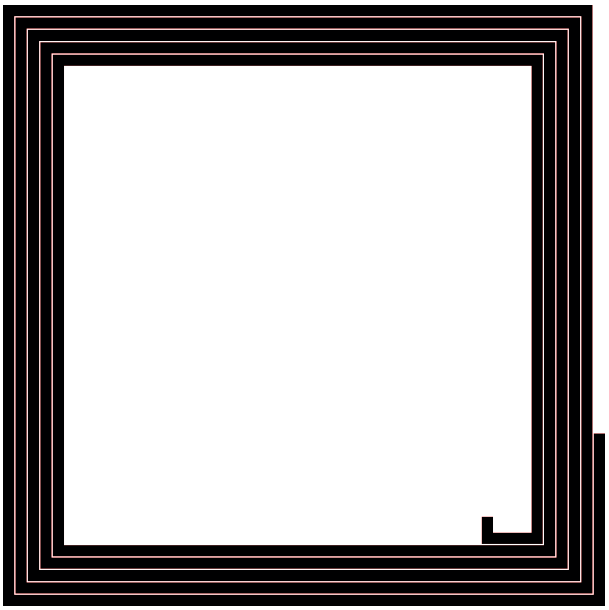

Figure 4: Chip coil with the dimensions specified in Table 3.

For comparison, the resulting power transfer efficiencies for the initial simulations, without adjusted geometries, for different frequencies are presented in Table 4.

5 Discussion

The simulation results presented in Section 4 show that it is possible to achieve power transfer efficiencies which are high enough to power the low-power monitoring system presented in the introduction. However, comparing the power transfer efficiency of this work, −34.7 dB, with the power transfer efficiency of the work of Zargham and Gulak [4], who achieve a measured power transfer efficiency of −20.15 dB at 187 MHz through 10 mm of bovine muscle reveals that other systems can achieve higher power transfer efficiencies.

Table 4: Power transfer efficiencies for initial simulations at different frequencies

Frequency [MHz]	40.66	169.4	433.0	868.0
Power transfer efficiency [dB]	-61.4	-41.4	-34.2	-37.6

In this section, we compare our results with those of [4] and comment on power transfer efficiency in general. The authors are not aware of other wireless power transfer systems for CMOS ICs which achieve similar power transfer efficiencies to those of Zargham and Gulak.

5.1 Conductive Media and Frequency

The intended application for the work of Zargham and Gulak is implantable chips in humans for medical purposes. Thus they report power transfer efficiencies through bovine muscle, which is more conductive than the silicone gels found in power semiconductor modules, which are insulators. As this conductivity increases with frequency, so do the conductive losses which explains the fact that our simulations resulted in a higher operating frequency than that of Zargham and Gulak. Another difference between the two works is that Zargham and Gulak allowed any operating frequency while we required for our work that the operating frequency lie within an ISM band. This requirement has both advantages and disadvantages. The obvious advantage of having the operating frequency in an ISM band is that the allowed radiated power is high compared to other bands and the requirement to shield the system may thus be removed. Another advantage is that the simulation time can be significantly reduced if the simulations need only to be carried out for select frequencies in contrast to be swept over a range of frequencies. A disadvantage is that limiting the available frequencies reduces the power transfer efficiency unless the optimal frequency occurs within an ISM band.

5.2 Low-power Operation

Zargham and Gulak evaluates power consumption assuming that a matching network can be designed which allows the wireless power transfer system to drive an optimal load. For our system we have assumed a 100 kΩ load, which is suitable if our proposed temperature monitoring system was to be realised. This limits the achievable power transfer efficiency because of the matching components required to drive such a load with optimal efficiency. Thus, we have evaluated the power transfer efficiency using only a capacitor in parallel to the load as a matching network. The possibility to manufacture components to drive an optimum load on a CMOS chip would have significantly increased the power transfer efficiency.

5.3 Power Transfer Efficiency

The total power transfer efficiency, η, can be divided into several components of power transfer efficiencies. The power transfer efficiency can be written as

$$\eta = \eta_{\text{source}} \cdot \eta_{\text{link}} \cdot \eta_{\text{matching}} \cdot \eta_{\text{rectifier}}, \tag{1}$$

where η_{source} is the power transfer efficiency of the power amplifier driving the PCB coil; η_{link} is the power transfer efficiency due of the wireless link and includes losses in the

media between the coils, the power lost due to radiation as well as the power lost due to resistive heating in the coils; η_{matching} is the power transfer efficiency of the matching network; and $\eta_{\text{rectifier}}$ is the power transfer efficiency of a rectifier placed before the load.

In this work, we have focused on optimising $\eta_{\text{link}} \cdot \eta_{\text{matching}}$ as these are the major contributors to losses for wireless power transfer systems to ICs. [9] has demonstrated a class E power amplifier with a power transfer efficiency of 89.5 % at 450 MHz, while [10] has demonstrated an active rectifier with a power transfer efficiency of 53.5 % at 100 MHz while arguing that it should be possible to design a rectifier with a power transfer efficiency of over 70 % for frequencies up to 600 MHz if certain challenges are overcome.

6 Conclusion

In this paper we present simulations which demonstrate a power transfer efficiency of −34.7 dB for a wireless power transfer system within a power semiconductor module constituting a transmitter PCB PSC to a receiver CMOS PSC separated by 10 mm. The intended application is a temperature monitoring system for power semiconductor modules which would enable the detection of emerging faults such as solder fatigue. The simulations show that it is feasible to construct a wireless power transfer system which provides sufficient power for a low-power CMOS temperature sensor to operate, such as the one demonstrated in [8]. For example, if 10 µW is required for the sensor, approximately 30 mW would have to be input to the wireless power transfer system. Taking into account the power transfer efficiencies of state-of-the-art high-frequency power amplifiers and rectifiers, approximately 62 mW would have been required.

Acknowledgement

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Paper E

Maximal Q Factor for an On-Chip, Fuse-Based Trimmable Capacitor

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Maximal Q Factor for an On-Chip, Fuse-Based Trimmable Capacitor

Joakim Nilsson, Johan Borg och Jonny Johansson

Abstract

This paper presents a circuit for realising a fuse-programmable capacitor on-chip. The trimming mechanism is implemented using integrated circuit fuses which can be blown in order to lower the resulting equivalent capacitance. However, for integrated circuits, the non-zero fuse resistance for active fuses and finite fuse resistance for blown fuses limit the Q factor of the resulting capacitor. In this work, we present a method on how to arrange the fuses in order to achieve maximal worst-case Q factor for the given circuit topology given the process parameters and requirements on capacitance. We also analyse and discuss the accuracy and limitations of the topology with regard to fuse resistance and parasitic elements such as bond pads.

1 Introduction

The goal to design resonant circuits for single-chip radio-frequency (RF) systems has created the need for trimmable [1] integrated circuit (IC) capacitors. Applications for such circuits exist in the field of wireless transfer of power directly to a single-chip system, where the RF inductor is integrated on the die. Examples of applications include implantable chips in humans for biomedical purposes [2, 3], and sensors for condition monitoring of power semiconductors, where a wireless power supply and communication interface provides galvanic isolation from the high-voltage power semiconductors [4, 5].

For both examples, the on-chip coils would be optimised based on the properties of the surrounding materials: tissue data [6] in the case for biomedical implants, and power semiconductor module geometry data [5] in the case for sensors for condition monitoring. In these types of application, a capacitor can be used to form a resonant circuit with the receiver on-chip coil, which boosts the voltage induced the in coil. However, for resonant circuits in single-chip systems such as described above, the obtained resonant frequency may deviate from the desired one because of large tolerances in the IC manufacturing process. Obtaining a specific frequency can be important for RF applications for which the frequency must lie within a frequency band which allows sufficient energy to be radiated, for example an industrial, scientific and medical (ISM) band [7]. Tunability is also important for applications where many devices must be powered by the same transmitter and thus operate at the same frequency. One way to adjust the resonant frequency is to trim the value of the capacitor in an LC circuit.

As an alternative to relatively costly laser-trimmed [8] IC capacitors, in this paper we discuss how to optimise fuse-based binary-weighted trimmable capacitors in order to maximise their Q factors which in turn will maximise the Q factors for any resonant circuits built from such capacitors. One such circuit could be an LC circuit consisting of an RF receiver coil and a resonant trimmable capacitor used for frequency tuning. The main issue we address is the effect of non-zero and finite resistance for active and blown IC fuses, respectively.

Although the theory presented in this work is valid not only for fuses, but also for semiconductor switches such as MOSFETs, this paper addresses only fuses. This decision is motivated by the fact that for applications which require a wireless power supply, no power source is available to bias a semiconductor into a desired switching state. Furthermore, even if semiconductors were to be used, such as in [9], effects from e.g. parasitic capacitance and temperature-dependent leakage current would still have to be taken into account.

Furthermore, because fuses are one-time programmable, if possible, we recommend using capacitive structures which have good temperature and bias stability such as metal-insulator-metal (MIM) capacitors [10], which also exhibit high Q factors. In contrast, using metal-oxide semiconductor field effect transistor (MOSFET) capacitors would introduce a strong dependence on bias for the resulting capacitance [11]. Furthermore, if no power source is available for bias, the MOSFETs would be biased in the region where the capacitance varies the most and the variation in capacitance with voltage would be extremely strong [11], defeating the purpose of trimming.

For biomedical implants, a concern could be that the impedance of an implanted coil would be sensitive to the electromagnetic properties of the surrounding tissue which are only known approximately and may change over time, which in turn would result in a change in resonant frequency. However, the encapsulation of the IC chip can be made comparable in size to the coil diameter, for example a $2 \times 2\,\mathrm{mm}^2$ chip with a 1 mm encapsulation. In such a case, the electromagnetic fields generated by the on-chip coil will extend mainly into the encapsulation material (whose electromagnetic properties are known to a high accuracy and do not change) and not into the surrounding tissue. Thus the resonance frequency can be trimmed before implantation and will not change over time.

The paper is organised as follows. In Section 2, we introduce the circuit and discuss how to optimise it for maximum Q factor and in Section 3 we discuss the accuracy of the optimised circuit. In Section 4, we present an example relating the theory to an application and discuss the results. The conclusion is presented in Section 5.

2 Trimmable Capacitor Bank

Consider the trimmable capacitor bank shown in Figure 1. The circuit comprises one base capacitor, C, in parallel with m binary-weighed trim capacitors, $C_0, C_1, ..., C_{m-1}$, distributed as $C_n = C_\mathrm{x}/2^n$. The trim capacitors can be deactivated by blowing their corresponding fuse in $\{F_0, F_1, ..., F_{m-1}\}$. The equivalent capacitance, C_eq, seen between

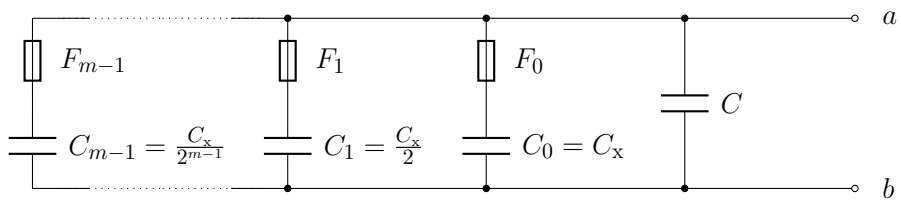


Figure 1: Fuse-based trimmable capacitor.

nodes a and b can be written as

$$C_{\text{eq}} = C + \sum_{n=0}^{m-1} F_n \frac{C_{\text{x}}}{2^n}, \tag{1}$$

where F_n is 0 if fuse n is blown and 1 if it is active. From Eq. (1), it can be seen that by letting F_n represent bit n of an m-bit binary number, C_{eq} can be controlled from C to $C + \Delta C$ with the resolution of the smallest trim capacitance, $C_{\text{res}} = C_{m-1} = C_{\text{x}}/2^{m-1}$. Because ΔC is the sum of all the trim capacitances, it can be written as

$$\Delta C = \sum_{n=0}^{m-1} \frac{C_{\text{x}}}{2^n}. \tag{2}$$

By solving Eq. (2) for C_{x}, we arrive at the following expression:

$$C_{\text{x}} = \frac{\Delta C}{2(1 - 1/2^m)}. \tag{3}$$

Thus, from the base capacitance, C, and trim capacitance, ΔC, needed for the application, values can be selected for all the capacitors in the circuit of Figure 1.

2.1 Finite / non-Zero Fuse Resistance

For ICs, both the fuse on-resistance, $R_{\text{f, on}}$, and off-resistance, $R_{\text{f, off}}$ can be significant. In many process technologies, a unit fuse is available with a fixed on- and off-resistance and for the examples in this work, values of $R_{\text{f, on}} = 25\,\Omega$ and $R_{\text{f, off}} = 80\,\text{k}\Omega$, relevant to a 180 nm process, are assumed. It is however possible to realise arbitrary on- and off-resistances, $r_{\text{f, on}}$ and $r_{\text{f, off}}$ by connecting a number of fuses in series and/or parallel and then either blowing all or none of the fuses in a branch. Because $R_{\text{f, on}}$ and $R_{\text{f, off}}$ are constant, the on-resistance of the resulting network will always be linearly related to its off-resistance by a factor,

$$k_{\text{f}} = \frac{R_{\text{f, on}}}{R_{\text{f, off}}} = \frac{r_{\text{f, on}}}{r_{\text{f, off}}}. \tag{4}$$

The question thus arises on how to select $r_{\text{f, on}}$ (or, equivalently $r_{\text{f, off}}$) in order to maximise the Q factor for the resulting capacitor for the worst-case configuration of active/blown fuses. It should be noted that both $R_{\text{f, on}}$ and $R_{\text{f, off}}$ is highly process dependent, which may make fuse trimming less attractive in some processes than others, particularly those in which k_{f} is small, which will be demonstrated later in this section.

2.2 Q Factor Optimisation for a Single Branch

Consider starting with the base capacitance, C, and adding a single fuse-controlled branch to that circuit. The resulting Q factor, $Q_{\mathrm{eq}}(a_{\mathrm{f}})$, for arbitrarily selected component values are plotted in Figure 2 as a function of the fuse scaling factor, a_{f}, with the fuse resistance, R_{f}, attaining values for both active and blown fuses. Here a_{f} is the factor by which a fuse is scaled by a series and/or parallel connection that gives a scaled fuse resistance $r_{\mathrm{f}} = a_{\mathrm{f}} R_{\mathrm{f}}$, and also $r_{\mathrm{f,\,on}} = a_{\mathrm{f}} R_{\mathrm{f,\,on}}$ and $r_{\mathrm{f,\,off}} = a_{\mathrm{f}} R_{\mathrm{off}}$. In order to maximise the resulting worst-case Q factor, we want to find the value of a_{f} for which the worst-case $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ for both cases of R_{f} is as large as possible. That is, we want to maximise the function

$$f(a_{\mathrm{f}}) = \min\left(Q_{\mathrm{eq}}(a_{\mathrm{f}})\Big|_{R_{\mathrm{f}}=R_{\mathrm{f,\,on}}}, Q_{\mathrm{eq}}(a_{\mathrm{f}})\Big|_{R_{\mathrm{f}}=R_{\mathrm{f,\,off}}} \right). \tag{5}$$

From the figure, it can be seen that the maximum Q_{eq} is obtained either for very small values for a_{f} or for very large values for a_{f}. In fact, Q_{eq} tends towards infinity for such values. The reason for this is that, for very small a_{f}, the fuse behaves as a short circuit for both its active and blown state and thus does not contribute significantly to the total equivalent resistance of the circuit. The contrary is true for very large a_{f}, where the fuse behaves as an open circuit for both cases and thus the branch does not contribute significantly to the equivalent impedance. Thus, if we choose such extreme values for a_{f}, the resulting equivalent capacitance can no longer be controlled by the fuse. Therefore, we must choose a value for a_{f} in a region where the fuse behaves as a short circuit for active fuses (to the left of the minimum $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ of the blue solid line), and as an open circuit for blown fuses (to the right of the minimum $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ for the red dashed line). It can be seen from Figure 2 that a local maximum for $f(a_{\mathrm{f}})$ within this region occurs at the intersection point of the of the curves representing the Q factor for $R_{\mathrm{f}} = R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f}} = R_{\mathrm{f,\,off}}$, respectively.

Note that this point represents the fuse resistances for which the Q factor has degraded equally for the active and blown states of the fuse. Deviating from this point increases the Q factor for one of these states, but decreases it for the other. The intersection point thus represents the highest possible worst-case Q factor for the equivalent capacitor. It should also be noted that Figure 2 assumes infinite Q factors for all involved capacitors. If IC capacitors can be manufactured with a Q factor of Q_{cap}, for extreme values for a_{f}, Q_{eq} would approach Q_{cap} asymptotically instead of tending towards infinity. In fact, this behaviour is shown in a lighter shade in the figure. The simplification is made because it is reasonable to assume that the series resistance contributed to one of the capacitors by a scaled fuse will be much larger than the equivalent series resistance (ESR) of the capacitor itself. Thus, for non-extreme values for a_{f}, which are the values we are interested in, Q_{cap} will be much larger than Q_{eq}.

In the pursuit to find an expression for the intersection point of Figure 2, consider the equivalent impedance, Z_{eq}, resulting from the parallel connection of two impedances, $Z_1 = R_1 + \mathrm{j}X_1$ and $Z_2 = R_2 + \mathrm{j}X_2$. Here, symbols R and X denote the resistance and reactance, respectively, of the impedance Z with corresponding index. It can be shown

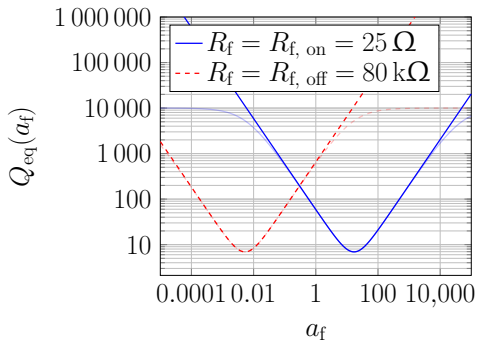


Figure 2: Q factor, $Q_{eq}(a_f)$, for a 3 pF capacitor in parallel with a series combination of a fuse and a 1 pF capacitor, plotted as a function of fuse scaling factor, a_f. $Q_{eq}(a_f)$ is plotted for both active and blown fuses corresponding to different fuse resistances. Plots for manufactured capacitors with both infinte Q factors and Q factors of 10 000 are shown, with the latter case in a lighter shade.

that Z_{eq} is given by

$$Z_{\text{eq}} = Z_1||Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2} = \frac{X_1\left(R_2^2 + X_2^2\right) + X_2\left(R_1^2 + X_1^2\right) + \text{j}\left[R_1\left(R_2^2 + X_2^2\right) + R_2\left(R_1^2 + X_1^2\right)\right]}{(R_1 + R_2)^2 + (X_1 + X_2)^2}. \tag{6}$$

Regarding the resulting impedance as a capacitor with a series resistance, the resulting Q factor is given by

$$Q_{\text{eq}} = -\frac{\Im\left\{Z_{\text{eq}}\right\}}{\Re\left\{Z_{\text{eq}}\right\}} = -\frac{X_1\left(R_2^2 + X_2^2\right) + X_2\left(R_1^2 + X_1^2\right)}{R_1\left(R_2^2 + X_2^2\right) + R_2\left(R_1^2 + X_1^2\right)}. \tag{7}$$

To find the intersection point of Figure 2 in terms of the scaled fuse resistance, $r_{\text{f, on}} = a_{\text{f}} R_{\text{f, on}}$, we set

$$Q_{\text{eq}}(a_{\text{f}})\Big|_{R_1 = r_{\text{f, on}}} = Q_{\text{eq}}(a_{\text{f}})\Big|_{R_1 = k_{\text{f}} r_{\text{f, on}}}, \tag{8}$$

where k_{f} is given by Eq. (4) and a_{f} is the scaling factor which can be obtained by a series and/or parallel connection of fuses. Substituting Eq. (7) into Eq. (8) yields

$$-\frac{X_1\left(R_2^2 + X_2^2\right) + X_2\left(r_{\text{f, on}}^2 + X_1^2\right)}{r_{\text{f, on}}\left(R_2^2 + X_2^2\right) + X_2\left(r_{\text{f, on}}^2 + X_1^2\right)} = -\frac{X_1\left(R_2^2 + X_2^2\right) + X_2\left(k_{\text{f}}^2 r_{\text{f, on}}^2 + X_1^2\right)}{k_{\text{f}} r_{\text{f, on}}\left(R_2^2 + X_2^2\right) + X_2\left(k_{\text{f}}^2 r_{\text{f, on}}^2 + X_1^2\right)} \tag{9}$$

Solving Eq. (9) for $r_{\text{f, on}}$ yields

$$r_{\text{f, on}} = R_2 \frac{1}{2k_{\text{f}}} \frac{X_1}{X_2} \pm \sqrt{\left(R_2 \frac{1}{2k_{\text{f}}} \frac{X_1}{X_2}\right)^2 + \frac{1}{k_{\text{f}}}\left(R_2^2 \frac{X_1}{X_2} + X_1 X_2 + X_1^2\right)}. \tag{10}$$

Relating this expression to Figure 1, we substitute $X_1 = -1/(\omega C_n)$, $X_2 = -1/(\omega C)$ and $R_2 = R$, where C_n is the added capacitance in the branch currently being added, C is the

base capacitance including all thus far added branches, R is the resistance in series with C resulting from all fuse resistances from all thus far added branches and ω is the angular frequency under which the circuit is intended to operate. Thus, $r_{\mathrm{f,\,on}}$ as a function of branch number, n, can be written as

$$r_{\mathrm{f,\,on}}(n) = R\frac{1}{2k_{\mathrm{f}}}\frac{C}{C_n} \pm \sqrt{\left(R\frac{1}{2k_{\mathrm{f}}}\frac{C}{C_n}\right)^2 + \frac{1}{k_{\mathrm{f}}}\left(R^2\frac{C}{C_n} + \frac{1}{\omega^2 C C_n} + \frac{1}{\omega^2 C_n^2}\right)}. \tag{11}$$

Let Q represent the Q factor given by the series combination of C and R. Then, $Q = 1/\omega CR$. Substituting this expression into Eq. (11) yields

$$r_{\mathrm{f,\,on}}(n) = R\frac{1}{2k_{\mathrm{f}}Q\omega C_n} \pm \sqrt{\left(\frac{1}{2k_{\mathrm{f}}Q\omega C_n}\right)^2 + \frac{1}{k_{\mathrm{f}}\omega C_n}\left[R\left(Q + \frac{1}{Q}\right) + \frac{1}{\omega C_n}\right]}. \tag{12}$$

For practical component values, the inequalities $Q \gg 1/Q$ and

$$2k_{\mathrm{f}}Q^2 \gg \frac{1}{R(Q + 1/Q)\omega C_n + 1} \tag{13}$$

hold and because $r_{\mathrm{f,\,on}} > 0$, Eq. (12) reduces to

$$r_{\mathrm{f,\,on}}(n) \approx \sqrt{\frac{1}{k_{\mathrm{f}}\omega C_n}\left(RQ + \frac{1}{\omega C_n}\right)} = \sqrt{\frac{1}{k_{\mathrm{f}}\omega C_n}\left(\frac{1}{\omega C} + \frac{1}{\omega C_n}\right)}. \tag{14}$$

Thus we have arrived at an expression for how to select the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$, when adding one fuse-controlled branch to the base capacitance.

2.3 Q Factor Optimisation for Multiple Branches

In order to find $r_{\mathrm{f,\,on}}(n)$ for the fuses in each branch, one possible solution is to use Eq. (14) recursively for all the branches. However, there is a challenge associated with this approach. Consider adding the first branch to the base capacitance. In this case, it is obvious which value to use for C. However, for the next branch, C might take on two different values depending on whether the fuse will be active or blown in the first branch, so we would also need to consider the case for when C is substituted for $C + \Delta C$. When adding the third branch, there will be four possible values for C. In fact, the number of values would double for each new branch added.

Because of this complexity, we do not pursue this approach further. Instead, we use Eq. (14) to obtain an expression for the Q factor, Q_n, of the branch being added when its fuse is active:

$$Q_n = \frac{1/\omega C_n}{r_{\mathrm{f,\,on}}(n)} = \sqrt{\frac{k_{\mathrm{f}}}{1 + \frac{C_n}{C}}}. \tag{15}$$

If only one branch would be added, we could use Eq. (15) to know which Q factor it should have in its active state, which would in turn yield a value for $r_{\mathrm{f,\,on}}(n)$. However, as

explained above, we don't know which value to use for C in the coming branches because the fuse configuration is unknown. Thus, it appears that we can only use Eq. (15) to find $r_{\mathrm{f,\,on}}(n)$ for one of the branches.

However, consider the case when all branches have the same Q factor with all fuses active. We denote this Q factor Q_{on}. The equivalent Q factor does not change if multiple branches with identical Q factor are connected in parallel. Therefore, for a certain fuse configuration, we would have one equivalent Q factor, Q_{on}, for all active branches and one equivalent Q factor, Q_{off}, for all blown branches. Because the Q factor is inversely proportional to the branch resistance, $Q_{\mathrm{on}} = k_{\mathrm{f}} Q_{\mathrm{off}}$. If we attempt to increase Q_{on} by increasing the Q factor for a single branch, the Q factor for that branch in its blown state will also increase. While this would result in an increased Q_{eq} for when this branch is active, it would decrease it for when it is blown. Refer to Figure 2 and note that at the intersection point, an increased Q_{on} would mean a decreased a_{f} and thus a decreased scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$. Following the blue solid line from the intersection point for decreasing a_{f} yields a higher Q_{eq}. However, for Q_{off}, following the red dashed line for decreasing a_{f} yields a lower Q_{eq}.

Similarly, we could try to increase the worst-case Q_{eq} by increasing Q_{off}. However, this would also increase it for Q_{on} and, by the same reasoning as before, would result in a lower worst-case Q_{eq}. Attempting to change the fuse resistance for multiple branches simultaneously will also not improve the worst-case Q_{eq} because for the worst-case, the fuse state resulting in the lowest Q_{eq} will be in use for each branch. Thus, we conclude that Q_{eq} will be maximised when all branches have the same Q factor. This Q factor can be found by considering the equivalent circuit for all branches with the fuses in their active state and then using Eq. (15) and substituting C_n for the equivalent parallel resistance for the branches, ΔC, to find the Q factor for a branch, $Q_{\mathrm{branch}} = Q_n$, for all n:

$$Q_{\mathrm{branch}} = \sqrt{\frac{k_{\mathrm{f}}}{1 + \frac{\Delta C}{C}}}. \tag{16}$$

Eqs. (16) and (15) can then be used to find $r_{\mathrm{f,\,on}}(n)$ as

$$r_{\mathrm{f,\,on}}(n) = \frac{1}{Q_{\mathrm{branch}}} \frac{1}{\omega C_n} = \frac{1}{Q_{\mathrm{branch}}} \frac{2^n}{\omega C_{\mathrm{x}}}. \tag{17}$$

This is an expression for the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$, for each branch, which yields the maximal worst-case equivalent Q factor, Q_{eq}. Here, $C_n = C_{\mathrm{x}}/2^n$ was used in order to obtain an expression for $r_{\mathrm{f,\,on}}(n)$ as a function of C_{x}. It should be noted that if the exact value for $r_{\mathrm{f,\,on}}(n)$ required by Eq. (17) cannot be obtained because a prohibitively large number of fuses would be required, an error will be introduced in Q_{branch}. Because the Q factor of a capacitor is given by its reactance divided by its resistance (that is, in the case for Q_{branch}, divided by $r_{\mathrm{f,\,on}}(n)$), the relative error in the worst-case Q_{branch} will be no greater than the relative worst-case error in $r_{\mathrm{f,\,on}}(n)$, or equivalently, no greater than the relative error in the fuse scaling factor, a_{f}, in the fuse with the largest relative scaling mismatch.

To obtain an expression for the resulting worst-case equivalent Q factor when a fuse-controlled branch is connected in parallel with the base capacitance, C, we use Eq. (7) and substitute

$$R_1 = r_{\text{f, on, eq}} = \frac{1}{Q_{\text{branch}}} \frac{1}{\omega \Delta C}, \tag{18}$$

$$R_2 = 0, \tag{19}$$

$$X_1 = \frac{1}{\omega \Delta C}, \tag{20}$$

$$X_2 = \frac{1}{\omega C}, \tag{21}$$

where $r_{\text{f, on, eq}}$ is the scaled fuse on-resistance obtained for a branch with ΔC as series capacitance. The resulting expression is given by

$$Q_{\text{eq}} = Q_{\text{branch}} \left(1 + \frac{C}{\Delta C}\right) + \frac{1}{Q_{\text{branch}}} \frac{C}{\Delta C}. \tag{22}$$

Inserting Eq. (16) into Eq. (22) and making the assumption that $Q_{\text{branch}} \gg 1$ yields

$$Q_{\text{eq}} \approx \left(1 + \frac{C}{\Delta C}\right) \sqrt{\frac{k_{\text{f}}}{1 + \frac{\Delta C}{C}}} = \sqrt{k_{\text{f}} \frac{(1 + C/\Delta C)^2}{1 + \Delta C/C}}. \tag{23}$$

From Eq. (23) it can be seen that increasing the ratio of base capacitance to trim capacitance, $C/\Delta C$, increases Q_{eq}. This is intuitive because that increases the ratio of capacitance contributed by capacitors with no series resistance to capacitance contributed by capacitors with series resistance. It can also be seen that a higher ratio, k_{f}, between off and on resistance for the fuses used will increase Q_{eq}, which is also intutive because higher quality fuses should yield better Q factors.

It is interesting to note that highest possible worst-case Q factor, Q_{eq}, depends only on the ratio between desired base and trim capacitance as well as on the ratio of resistance between blown and active fuses for the process technology and is thus frequency-independent.

3 Capacitance Accuracy

Because C_{eq} is the result of connecting a capacitor with no series resistance in parallel to a number of capacitors with series resistance, the resulting capacitance value will not be exactly equal to the target capacitance. Another contribution to the mismatch in capacitance comes from parasitic elements such as bond pads used to program (blow) the fuses. In this section, we quantify these mismatches.

3.1 Effects of Fuse Resistance

Consider adding a single branch to the base capacitance, C. If the fuse for that branch is active, the contributed capacitance will be slightly lower than the actual value of the capacitor in that branch, C_n, because of the series resistance of the branch. On the other hand, if the fuse for that branch is blown, the intent is that no capacitance should be contributed, but because of the finite fuse resistance, indeed some capacitance will be contributed. Thus, we see that active branches contribute too little capacitance, whereas blown branches contribute too much capacitance. The magnitude of the mismatch of target capacitance to actual capacitance will thus be largest either for all fuses active or for all fuses blown.

For the case for all fuses active, the equivalent impedance, Z_{eq}, can be found from Eq. (6). Since we are only interested in the difference in *capacitance*, we are only interested in the reactive part of Z_{eq}. Using the substitutions in Equations (18), (19), (20) and (21), it can be shown that the reactive part of Z_{eq} is given by

$$\hat{X}_{\text{eq}} = -\frac{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)\frac{1}{\omega\Delta C}+\frac{1}{\omega C}}{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)\frac{C}{\Delta C}+\frac{\Delta C}{C}+2}. \tag{24}$$

The maximum difference between the target capacitance, $(C+\Delta C)$, and the capacitance contributed by $\hat{X}_{\text{eq}}$ is given by

$$\hat{C}_{\text{error}} = (C+\Delta C) - \left(-\frac{1}{\omega \hat{X}_{\text{eq}}}\right). \tag{25}$$

Substituting Eq. (24) into Eq. (25) yields, after some algebra,

$$\hat{C}_{\text{error}} = \frac{1}{Q_{\text{branch}}^2+1}\frac{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)C\cdot\Delta C}{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)C+\Delta C}, \tag{26}$$

which for $Q_{\text{branch}}^2 \gg 1$ reduces to

$$\hat{C}_{\text{error}} \approx \frac{1}{Q_{\text{branch}}^2}\frac{C\cdot\Delta C}{C+\Delta C}. \tag{27}$$

Thus, we have arrived at an expression for the maximum error in capacitance, $\hat{C}_{\text{error}}$, for all fuses active. It is interesting to note that Eq. (27) can be interpreted as follows: The maximum error in capacitance equals the equivalent capacitance of two series-connected capacitors of capacitance C and ΔC, respectively, scaled by the factor $1/Q_{\text{branch}}^2$.

An expression for for the equivalent reactance for the case for all fuses blown, here denoted $\check{X}_{\text{eq}}$, can be obtained from Eq. (6) using the substitutions in Equations (19), (20) and (21), and substituting

$$R_1 = k_{\text{f}} r_{\text{f, on, eq}} = \frac{k_{\text{f}}}{Q_{\text{branch}}}\frac{1}{\omega\Delta C}. \tag{28}$$

Utilising Eq. (16) and solving for k_f, $\check{X}_\mathrm{eq}$ is given as

$$\check{X}_\mathrm{eq} = -\frac{\left[1+Q_\mathrm{branch}^2\left(1+\frac{\Delta C}{C}\right)\right]\frac{1}{\omega\Delta C}+\frac{1}{\omega C}}{\left[1+Q_\mathrm{branch}^2\left(1+\frac{\Delta C}{C}\right)\right]\frac{C}{\Delta C}+\frac{\Delta C}{C}+2}. \tag{29}$$

The maximum difference between the target capacitance, C, and the capacitance contributed by $\check{X}_\mathrm{eq}$ is given by

$$\check{C}_\mathrm{error} = C - \left(-\frac{1}{\omega\check{X}_\mathrm{eq}}\right). \tag{30}$$

It can be shown that substituting Eq. (29) into Eq. (30) yields

$$\check{C}_\mathrm{error} = -\frac{1}{Q_\mathrm{branch}^2+1}\frac{\left(1+\frac{1}{Q_\mathrm{branch}^2}\right)C\cdot\Delta C}{\left(1+\frac{1}{Q_\mathrm{branch}^2}\right)C+\Delta C}, \tag{31}$$

which is exactly equal in magnitude to $\hat{C}_\mathrm{error}$ in Eq. (26), but with opposite sign; $\check{C}_\mathrm{error} = -\hat{C}_\mathrm{error}$. The error in capacitance for any fuse configuration, C_error, will thus lie within the interval

$$-\hat{C}_\mathrm{error} \leq C_\mathrm{error} \leq \hat{C}_\mathrm{error}. \tag{32}$$

In assessing the accuracy we have neglected the effects of capacitance variations with respect to process, voltage and temperature. As stated in the introduction, we recommend using MIM capacitors to realise the trim capacitor presented in this work because of their temperature and voltage stability [10]. However, the capacitors will still be subject some variation, especially as a result of variations in the manufacturing process. Because fuses are one-time programmable, they can not be used to compensate for variations in temperature or voltage which change over time, but they can be used to compensate for process variation. As an example, consider the application of an LC resonator discussed in the introduction. If the low-frequency inductance and the untrimmed resonant frequency are measured, the base capacitance, C, can be estimated from the resonance equation:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \tag{33}$$

where f_0 is the resonant frequency and L is the inductance of the resonator. When C is known, Eq. (33) can be used again to calculate the value needed for the trim capacitance, ΔC, in order to realise the desired value for f_0. If care is taken when designing the chip layout, the variations between C and ΔC can be matched to a high degree of accuracy and thus by estimating C, an estimation for ΔC can also be obtained.

However, if the on-chip inductance can not be measured with sufficient accuracy or if the parasitic capacitance of the inductive element is significant, a two-step (or multi-step) procedure could be performed in order to estimate values for the reactive elements. One measurement of f_0 could be taken before fuse-programming and a second one after

blowing the most significant fuse, F_0. Then, a least-squares approximation could be performed in order to obtain estimations of the sought values. However, for this case, because F_0 is used for parameter estimations instead of for trimming, the Q factor of the resulting capacitor would decrease compared to a single-step estimation procedure.

3.2 Parasitic Bond Pad Capacitance

To program (blow) a fuse, a large current is required. The current can be supplied through probe needles touching bond-pads on both sides of a fuse during factory testing. However, because bond-pads typically present a parasitic capacitance to ground on the order of hundreds of femtofarads, they can be an obstacle for the accuracy of the trimmable capacitor. This effect becomes significant when the bond pad capacitance becomes comparable to the smallest capacitor in the circuit, $C_{m-1} = C_x/2^{m-1}$. Note also that if a fuse consists of multiple fuses in series, an additional bond pad will be required for each series connection in order to be able to blow every fuse.

If a higher resolution is required than what a bond pad-based system can provide, probe pads could be used instead. Probe pads can typically be made small enough to present a parasitic capacitance to ground of the order of only a few femtofarads.

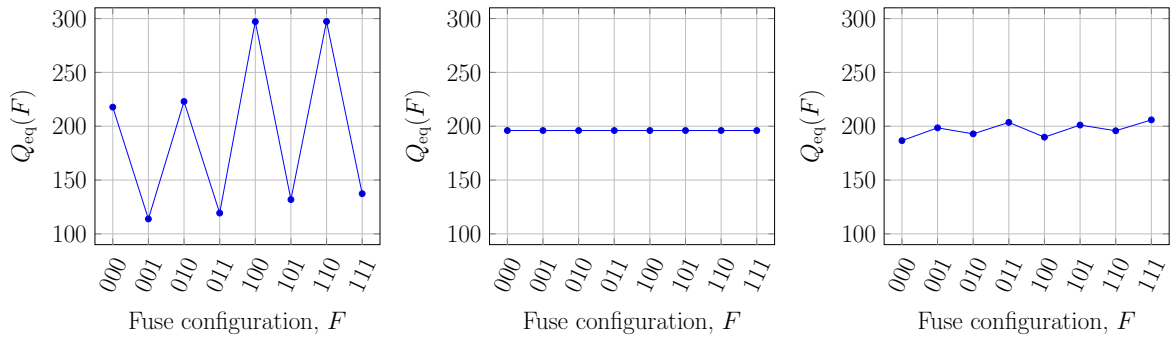
Another possibility is to let the programming of fuses be controlled by transistors. However, the ratio of capacitance to current-driving capability of transistors as well as the current required to blow a fuse is very dependent on process technology, and thus we do not attempt to assess the viability of this idea further in this work.

4 Discussion and Examples

In this section we discuss the performance of the circuit of this work by relating it to an example application.

Consider an application where we need a base capacitance, C, of 3 pF and a trim capacitance, ΔC, of 1 pF with a 3-bit resolution and at an operating frequency of 433 MHz. We thus use the circuit in Figure 1 and choose $C_\mathrm{x} = 571\,\mathrm{fF}$ according to Eq. (3). The resolution is thus $C_\mathrm{res} = C_2 = C_\mathrm{x}/2^2 = 143\,\mathrm{fF}$. The question arises on how to select the scaled fuse resistance for the different fuses, $r_{\mathrm{f,\,on}}(n)$. Consider first the naive design in which all fuses have the same resistance and consist only of a single fuse whose resistance is $R_{\mathrm{f,\,on}} = 25\,\Omega$ while active and $R_{\mathrm{f,\,off}} = 80\,\mathrm{k}\Omega$ while blown. Figure 3a shows the resulting equivalent Q factor, $Q_\mathrm{eq}(F)$, as a function of fuse configuration, F. Here, F is represented by a 3-bit binary number where 1 signifies an active fuse and 0 signifies that a fuse is blown. While the best-case Q factor is high at $Q_\mathrm{eq}(110) = 297$, the worst-case Q factor is much lower at $Q_\mathrm{eq}(001) = 114$.

A more balanced equivalent Q factor can be achieved if Eqs. (16) and (17) are used to obtain an expression for the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$. Using these equations, we



(a) Naive design (b) Ideal design (c) Practical design

Figure 3: Equivalent Q factor, $Q_{eq}(F)$, of a trimmable capacitor of $C = 3\,\text{pF}$ and $\Delta C = 1\,\text{pF}$, operating at 433 MHz as a function of the configuration of 3 fuses, represented by a binary number, F, where the nth bit represents fuse n, F_n. $F_n = 1$ signifies an active fuse, while $F_n = 0$ signifies that fuse n is blown. Plots are shown for three designs: (a) The naive design, where all fuses have the same resistance, R_f; (b) The ideal design, where all fuses have been scaled to their optimal resistance $r_f = a_f R_f$; and (c) The practical design, where all the fuses consist of series/parallel combinations of one or two fuses of resistance R_f in order to approximate $r_{f,\,on}$.

get

$$r_{\text{f}}(0) = 13.13\,\Omega, \tag{34}$$

$$r_{\text{f}}(1) = 26.26\,\Omega, \tag{35}$$

$$r_{\text{f}}(2) = 52.52\,\Omega. \tag{36}$$

Figure 3b shows the resulting Q factor, $Q_{\text{eq}}(F)$, as a function of F. It can be seen from the figure that the Q factor is constant independent of fuse configuration and that the worst-case Q factor has been increased to $Q_{\text{eq}}(F) = 196$, a 72 % increase compared to the naive design. Note that, as expected, this value for Q_{eq} coincides with the value at the intersection point of Figure 2.

The improvement results from the fact that we have identified that some configurations yield a much higher Q factor than others and made appropriate adjustments. By sacrificing the Q factor of the good configurations we have increased it for the worse ones resulting in a better Q factor for the worst case. The variation of the Q factor from 114 to 297 has been reduced to no variation at all.

Because of the potential high fuse count, it may be impractical to realise the values for $r_{\text{f},\,\text{on}}(n)$ in Eqs. (34), (35) and (36) to a high degree of accuracy with a series/parallel combination of a single fuse resistance, $R_{\text{f},\,\text{on}}$. However, the following combinations yield

values that are within 6 % of the desired ones using only one or two fuses for each branch:

$$r_{\mathrm{f,\,on}}(0) = (25\,\Omega)||(25\,\Omega) = 12.5\,\Omega, \tag{37}$$

$$r_{\mathrm{f,\,on}}(1) = 25\,\Omega, \tag{38}$$

$$r_{\mathrm{f,\,on}}(2) = 25\,\Omega + 25\,\Omega = 50\,\Omega. \tag{39}$$

Figure 3c shows the resulting equivalent Q factor, $Q_{\mathrm{eq}}(F)$. The worst-case value has now decreased to $Q_{\mathrm{eq}}(000) = 187$, a 5 % decrease compared to the ideal design. A result of this deviation from the ideal is that the Q factor is once again not completely constant.

The number of bond pads required to be able to blow all fuses amounts to 6 because there are a total of 5 fuses in the circuit and one additional bond pad for the current return path is required. Standard-size bond pads for a 180 nm process present a capacitance to ground around of 140 fF per pad. The total amount of capacitance from bond pads would thus be much larger than $C_{\mathrm{res}} = 143\,\mathrm{fF}$ and we would need to consider a different approach. Scaling down the pad area to $10 \times 10\ \mu\mathrm{m}^2$, probe pads with a capacitance of approximately 3.5 fF per pad can be manufactured. Using such pads to program the fuses results in a total parasitic capacitance contribution from pads of maximum 21 fF, which is about a factor of 7 smaller than the resolution, C_{res}. The variation in capacitance due to the non-ideal Q factors of the trim branches amounts to 344 aF, close to the ideal case of 312 aF, calculated from Eq. (26), which is far below the intended resolution.

In the previous example, the worst-case Q factor for the naive design is smaller than that for the practical design, however, not by a huge factor. This is because the process parameters, $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$, the desired base and trim capacitances, C and ΔC, number of bits, m, as well as the operating frequency happen to be of values which are beneficial for high Q factors. Consider what would happen if both specified capacitances, C and ΔC, are decreased by a factor of 10. Eqs. (16) and (17) show that significantly larger values would be needed for the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$. Figure 4 shows the equivalent Q factor, $Q_{\mathrm{eq}}(F)$, as a function of fuse configuration, F, for $C = 300\,\mathrm{fF}$ and $\Delta C = 100\,\mathrm{fF}$. Interestingly, identical graphs would be produced if either the operating frequency or $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$ were decreased by a factor of 10 instead of C and ΔC. From the figure, it can be seen that the fuse configuration $F = 111$ achieves a much more favourable Q factor than the other configurations, with $Q_{\mathrm{eq}}(111) = 1370$. The worst-case Q factor is significantly lower at $Q_{\mathrm{eq}}(000) = 22.9$. Relating to Figure 2, the reason for this behaviour is that the fuse scaling factor, a_{f}, for each fuse is not high enough and the operating point ends up to the left of the intersection point yielding very high Q factors for active fuses, but very low ones for blown fuses. Coming back to Figure 4, we see that only the case for all fuses active yields a high Q factor. By scaling the fuses appropriately and because the maximum worst-case Q factor is frequency-independent and constant for constant $k_{\mathrm{f}} = R_{\mathrm{f,\,off}}/R_{\mathrm{f,\,on}}$ and $\Delta C/C$, we can again achieve the Q factors of Figure 3b with a worst-case (and best-case) Q factor of $Q_{\mathrm{eq}}(F) = 196$.

To illustrate what could happen if care is not taken to ensure a sufficiently high Q factor, consider what would happen if a state-of-the art coil was to be used with the capacitor from the last example to form an LC resonator. Q factors of on-chip coils of

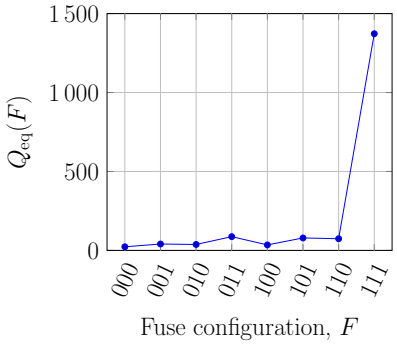


Figure 4: Equivalent Q factor, $Q_{eq}(F)$, of a trimmable capacitor as a function of the configuration of 3 fuses with the same resistance, R_f. All parameters are the same as in Figure 3a, except the specified capacitances, C and ΔC, have both been decreased by a factor of 10.

11.05 [2] and 10.5 [3] operating at hundreds of MHz have been demonstrated. Connecting one such coil to a capacitor with a worst-case Q factor of 22.9, as in the example, the worst-case Q factor of the resulting LC circuit would be reduced by over 30 % compared to the original Q factor of the coil. However, if the method described in this work was to be used, the coils could be connected to a capacitor with a worst-case Q factor of 187 as in Figure 3c, reducing the worst-case Q factor of the resulting LC circuit by less than 6 %.

Another challenge arises when we attempt to implement a practical circuit approximating the ideal design for this case of smaller capacitances. For instance, the highest resistance we would need to realise is $R_2 = 525\,\mathrm{k\Omega}$ for which 21 fuses would be needed. Such a circuit would require around 40 bond or probe pads which would present a relatively large parasitic pad capacitance, 140 fF in the worst case, to the trim capacitor, limiting the resolution. Since the desired resolution is even less than that at 100 fF, the circuit designers should consider accepting a lower resolution, reducing the number of bits and/or reducing the base capacitance, C.

The requirement of high numbers of series fuses arises when the largest scaled fuse resistance, $r_{\mathrm{f,\,on}}(m-1)$, becomes much larger than $R_{\mathrm{f,\,on}}$. Eqs. (16) and (17) show that this occurs when

$$\frac{2^{m-1}}{\omega C_{\mathrm{x}}}\sqrt{\frac{1+\frac{\Delta C}{C}}{k_{\mathrm{f}}}} \gg R_{\mathrm{f,\,on}}. \tag{40}$$

Thus, for higher frequencies, larger specified capacitances, larger fuse resistances or a fewer number of bits than for the previous example, a high number of series fuses would not be an issue. In this case, most fuses will be required in parallel instead, to achieve sufficiently low values for $r_{\mathrm{f,\,on}}(n)$.

5 Conclusion

In this paper, we present a circuit implementing a fuse-based IC trimmable capacitor. A theory is presented on how to choose fuse resistances in order to achieve the highest possible worst-case Q factor for the capacitor. One advantage of a fused-based approach is that it is cheaper than the alternative method of laser trimming. The theory presented in this work is novel in that, to the authors' knowledge, high-Q, fuse-based trimmable IC capacitors have not previously been published.

We show that proper selection of fuse resistances not only maximises the worst-case Q factor, but also makes it constant and independent of fuse configuration. This makes it possible to build applications such as on-chip tunable LC resonant circuits with a predictable Q factor that is independent of tuned frequency without resorting to laser trimming.

Furthermore the accuracy of the capacitance is discussed and it is concluded that capacitance from bond pads may be a limiting factor. This limitation can to some extent be overcome by the use of smaller, low capacitance probe pads.

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Paper F

Load-Dependent Power Transfer Efficiency for On-Chip Coils

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Load-Dependent Power Transfer Efficiency for On-Chip Coils

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Abstract

This paper presents a theory for the power transfer efficiency of printed circuit board coils to integrated circuit coils, with focus on load-dependence for low-power single-chip systems. The theory is verified with electromagnetic simulations modelled on a 350 nm CMOS process which in turn are verified by measurements on manufactured integrated circuits. The power transfer efficiency is evaluated by on-chip rectification of a 151 MHz signal transmitted by a spiral coil on a printed circuit board at 10 mm of separation to an on-chip coil. Such an approach avoids the influence of off-chip parasitic elements such as bond wires, which would reduce the accuracy of the evaluation.

It is found that there is a lower limit for the load below which reducing the power consumption of on-chip circuits yield no increase in voltage generated at the load. For the examined process technology, this limit appears to lie around 10 kΩ. The paper is focused on the analysis and verification of the theory behind this limit.

We relate the results presented in this work to the application of wireless single-chip temperature monitoring of power semiconductors and conclude that such a system is compatible with this limit.

1 Introduction

On-chip coils for wireless power transmission can be used to enable battery-free operation for integrated circuit systems such as implantable chips in humans [1, 2] as well as for galvanically isolated, direct-contact temperature sensors for condition monitoring of power semiconductors [3, 4]. For integrated circuits powered by on-chip coils, it is important to achieve a sufficiently high power transfer efficiency (PTE), so that on-chip sensors' power requirements can be met without an excessive amount of power being consumed at the transmitter. However, the small dimensions of an on-chip coil limit its ability to draw energy from a magnetic field generated by a transmitter coil. Another limiting factor for the PTE is the typically low Q factors for such coils, resulting in a high amount of resistive losses occurring in the coils. For example, Zargham and Gulak [1], and Feng *et al* [2] demonstrate on-chip coils with Q factors of 11.05 at 101 MHz and 10.5 at 450.3 MHz. This is in contrast to printed circuit board (PCB) coils for which it has been demonstrated that their Q factors can exceed 100 or even 400 if advanced PCB substrates are employed [5].

One additional challenge is the load requirements and the limitations imposed by the associated on-chip matching network. Because large integrated circuit (IC) inductors

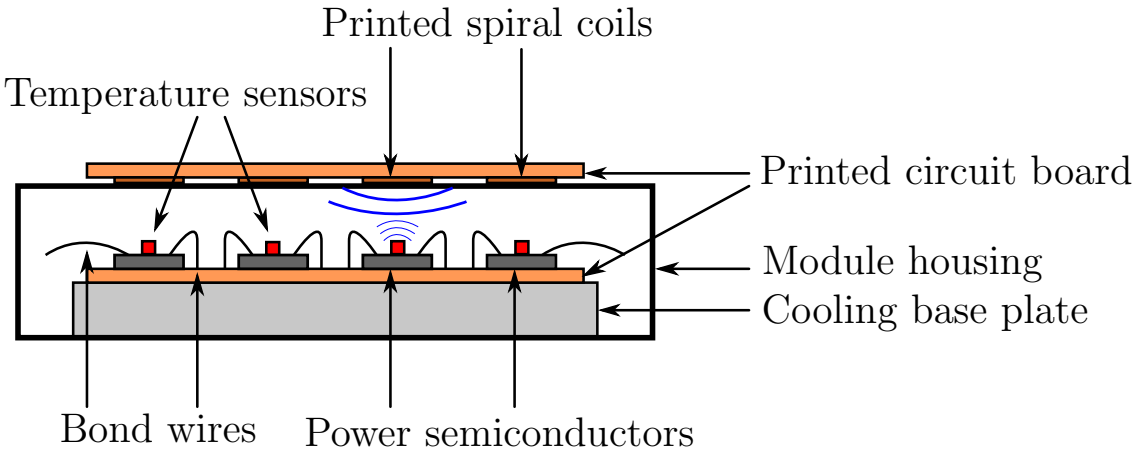

Figure 1: Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by printed spiral coils mounted on top of the module.

are difficult to manufacture with high Q factors, the matching network typically consists only of capacitors. Therefore any inductive part required by a matching network has to come from the on-chip receiver (Rx) coil. Because large load resistances require large inductors in order to be matched to the coil impedance, attempting to reduce the power consumption by reducing the load becomes ineffective beyond a certain point.

In this paper, we analyse the power transfer efficiency of systems powering on-chip coils with emphasis on the implications light loads (large load resistances) have on coil design. Focus is put on the implications for the power requirements of the transmitter. We evaluate the PTE by providing simulations for coil designs optimised for different loads and frequencies. In order to verify the simulation model, results of measurements are presented on an IC with an on-chip coil operating at 151 MHz complete with a simple single-transistor half-wave rectifier. The on-chip rectification approach enables accurate measurements to be made at the Rx side, because off-chip parasitic elements such as bond wires, probes and breakout tracks—which can be very significant at the frequency in question—are made irrelevant because off-chip currents are direct current (DC).

We assess the usefulness of the results presented in this work by relating them to the application of using wireless single-chip sensors to monitor the temperature of power semiconductors in a power semiconductor module, originally proposed in [3]. A schematic view of the proposed monitoring system is shown in Figure 1. Single-chip temperature sensors with on-chip coils are glued in direct contact with the power semiconductors to provide accurate temperature measurements in order to predict emerging faults. The sensors are powered by and communicates with printed spiral coils (PSCs) located on a PCB on top of the power semiconductor module. The wireless interface provides galvanic isolation between IC sensors and a system controller located on the PCB outside the module housing. Monitoring of temperature can be used to predict solder fatigue [6], bond wire lift-off [7] or be a part in predicting emerging semiconductor faults [8, 9]. In total, these faults account for 34 % of total failures in power electronic equipment [10].

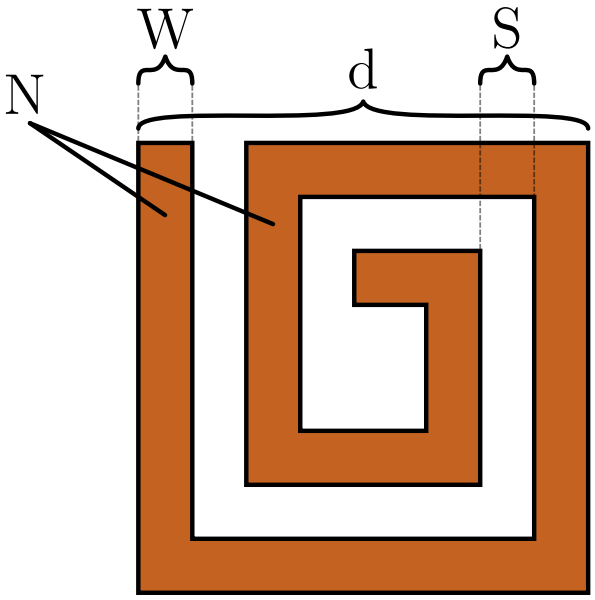

Figure 2: Schematic diagram of a printed spiral coil. Shown are the geometry parameters, tracewidth, W; trace separation, S; outer diameter, d; and number of turns, N used to describe its geometry.

The paper is organised as follows. In Section 2, we present an overview of how the power transfer efficiency is evaluated, including the measurement set-up and the placement of the different coils. In Section 3, we detail the circuits used to model the coils and derive a theoretical limit for for when the required transmitter power does not decrease even if the power consumption at the load is reduced. Section 4 presents simulations of optimised coil geometries supporting the theory. These simulations are verified by measurements on manufactured devices and the results of the measurements are presented in Section 5. Conclusions are presented in Section 6.

2 System Overview

In this section, we describe the measurement set-up used to evaluate the power transfer efficiency between two coupled coils: a transmitter (Tx) spiral coil printed on a PCB and an Rx spiral coil printed on an IC chip utilising a 350 nm complementary metal-oxide semiconductor (CMOS) process. The measurements are used to verify the simulation model presented in Section 4. Both Tx and Rx coils are PSCs characterised by outer dimension, d_{XX}; trace width, W_{XX}; trace separation, S_{XX}; and number of turns, N_{XX}. Here, XX denotes either the receiver coil, Rx, or the transmitter coil, Tx. These parameters are illustrated in the schematic diagram of Figure 2. The power transfer efficiency is evaluated at a coil separation of $D = 10\,\mathrm{mm}$, which is a reasonable distance both for biomedically implanted chips [1] and for sensor chips for condition monitoring of power semiconductors [4].

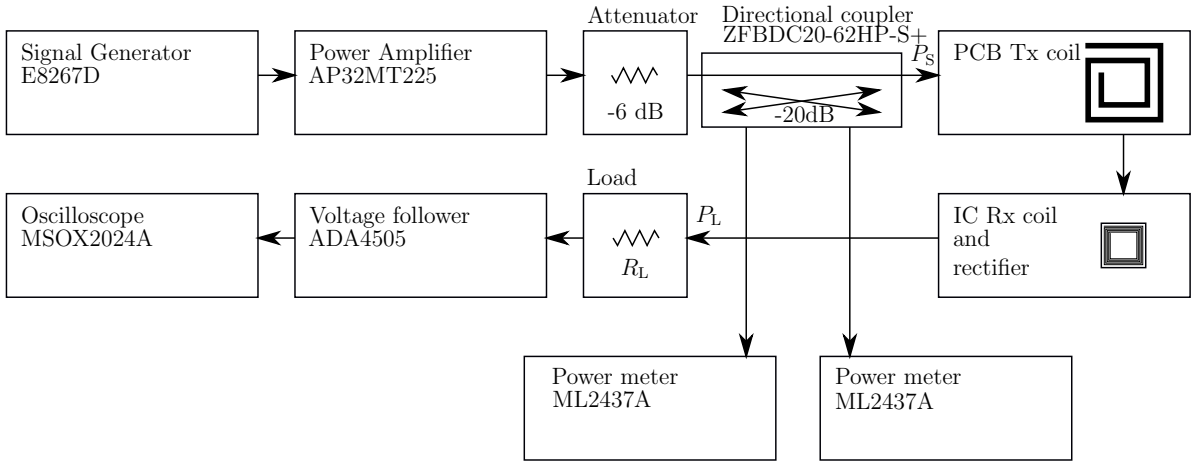

Figure 3: Overview of the measurement set-up used to verify the electromagnetic model used for simulations. A sinusiodal E8267D signal generator drives a APT32MT225 power amplifier. The signal is then attenuated by 6 dB *and the attenuated signal is fed to a ZFBDC20-62HP-S+ directional coupler from which* −20 dB *is coupled to and measured by an ML2437A power meter. The output of the coupler is fed to the PCB Tx coil and any reflected signal is fed back to the directional coupler and* −20 dB *of the reflected signal is measured by another ML2437A power meter. Power is transfer inductively from the PCB Tx coil to the IC Rx coil where the signal is rectified and fed to a load. The voltage at the load is buffered by an ADA4505 operational amplifier in voltage follower configuration and then sampled by an MSOX2024A oscilloscope.*

An overview of the measurement set-up is shown in Figure 3. The excitation signal is generated using a Prâna APT32MT225 Power Amplifer driven by a sinusoid which is generated by an Agilent E8267D Signal Generator. The power signal is attenuated by 6 dB by a power attenuator and the attenuated signal is fed to a Mini-Circuits ZFBDC20-62HP-S+ directional coupler from which −20 dB is coupled to and measured by an Anritsu ML2437A power meter. The output of the coupler is fed to a PCB with the Tx coil. Any reflected power from the PCB is fed back to the directional coupler from which −20 dB is coupled to another ML2437A power meter. Using the two power measurements, the power, P_S, delivered to the PCB can be calculated.

An inductive link is formed by the two coils, and a fraction of the signal power fed to the Tx coil is coupled to the Rx coil. In the following, this situation is described in more detail:

2.1 Transmitter Printed Circuit Board

On the Tx side, a PSC is printed on a PCB with a discrete LC matching network to enable sufficient power to be delivered to the Tx coil at the operating frequency. The matching network consists of a series variable capacitor and a shunt inductor. Because of the low equivalent series resistance (ESR) of the transmitting coil, losses in the matching components may be significant.

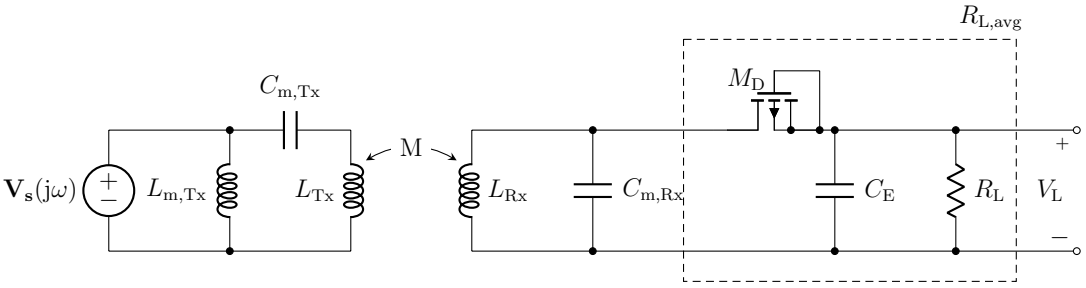

Figure 4: Schematic diagram of a PCB coil inductively coupled to a IC coil with on-chip single-transistor rectifier. The schematic also includes matching components and load resistance.

2.2 Receiver Chip

On the Rx side, a PSC is printed on an IC chip. Because large on-chip inductors require large area and typically exhibit low Q factors, the matching network consists of a single on-chip shunt capacitor, which forms a resonant circuit with the Rx inductor.

The integrated circuit includes a single-transistor half-wave rectifier, the purpose of which is to increase the accuracy of the measurements by rectifying on-chip and thus making the system less sensitive to parasitic effects. Such effects include magnetic coupling from the Tx coil to bond wires and PCB tracks as well as parasitic capacitance between such elements and within coaxial cable connectors. The simplicity of a single-transistor rectifier enables accurate estimation of its power consumption. It is thus possible to separate the power consumed in the rectifier from the power consumed in the load, P_{L}, obtaining estimations of both.

2.3 Inductive Link and Rectification

A circuit diagram of the two coupled Tx and Rx coils is shown in Figure 4 complete with matching networks, rectifier and load. An inductive link is formed between the Tx coil, L_{Tx}, and the Rx coil, L_{Rx}, coupled by the mutual inductance, M. $L_{\mathrm{m,Tx}}$ and $C_{\mathrm{m,Tx}}$ constitute the matching network on the Tx side while the single shunt capacitor, $C_{\mathrm{m,Rx}}$, constitutes the matching network on the Rx side. The metal-oxide semiconductor field effect transistor (MOSFET), M_{D}, is configured as a PMOS diode which rectifies the voltage induced in L_{Rx}. The rectified energy is used to drive a load resistor, R_{L}, external to the chip. Energy not consumed in the load is stored in the energy-storage capacitor, C_{E}, and used to drive the load when M_{D} is reverse-biased. Also shown is the equivalent resistance, $R_{\mathrm{L,avg}}$, due to the average loading of coil with matching network, which is the sum of R_{L} and the average equivalent resistance of the rectifier. The DC value of the load voltage, V_{L}, is buffered by an Analog Devices ADA4505 operational amplifier in voltage follower configuration and then sampled by an Agilent MSOX2024A oscilloscope. With the sampled voltage, the power, P_{L}, consumed at the load can be estimated.

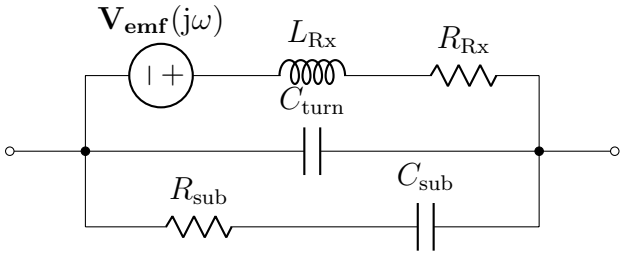

Figure 5: Ciruit used to model an on-chip coil.

3 Coil Modelling and Design

In this section we describe the electromagnetic situation for the monitoring system shown in Figure 1. A theory is presented demonstrating the effect that the loading of the on-chip coil has on transmitter power consumption. We argue that decreasing the load (that is increasing the load resistance) beyond a certain point has a negative impact on the power transfer efficiency which precisely cancels out the positive effect of a lower current consumption at the load. The result is that, beyond this point, the transmitter power required in order to realise a constant voltage at the load does not decrease even if the load is reduced.

In Section 4, we present simulation results to support the theory. These results are obtained from an optimisation algorithm that uses an electromagnetic simulator that generates optimised coil-designs for varying loads and frequencies.

3.1 On-Chip Coil Circuit Model

The on-chip coil is modelled as in Figure 5. Here, $\mathbf{V_{emf}}(\mathrm{j}\omega)$ is the electromotive force (emf) voltage phasor induced in the Rx coil from the magnetic field generated by the Tx coil. L_{Rx} is the coil inductance and R_{Rx} is the ESR of the coil due to the combined effects of non-zero resistance of the metal constituting the coil and due to resistive losses in the silicon substrate due to induced substrate current (and current induced in a substrate shield). C_{sub} and R_{sub} represent equivalent capacitance and resistance due to capacitive coupling to the ground-connected conductive substrate while C_{turn} represents the equivalent capacitance between turns. This is a simplified model whose purpose is to yield design insight of how the coil geometry affects the properties of the final coil.

The dependencies of the Rx model parameters, V_{emf}, R_{Rx}, L_{Rx}, R_{sub}, C_{sub} and C_{turn} on the Rx geometry parameters, W_{Rx}, S_{Rx} and N_{Rx} are summarised in Table 1. Here, V_{emf} is the amplitude of the emf voltage phasor, $\mathbf{V_{emf}}(\mathrm{j}\omega)$.

For thin, long conductors, the inductance increases with the logarithm of W_{Rx} [11], while the ESR decreases inversely proportional to W_{Rx}. The skin effect is assumed negligible because of the small thickness of the IC metal layers. Because of the increase in total surface-area consumed by the coil, increasing W_{Rx} results in that the coil will be capacitively coupled to a larger fraction of the substrate, decreasing R_{sub} and increasing C_{sub}. S_{Rx} has a similar effect on R_{sub} and C_{sub} due to increasing coil area, while also

Table 1: Model parameter dependencies on geometry parameters. Here, "-" denotes no or insignificant dependence, ↗ denotes a function that increases with the geometry parameter, while ↘ denotes a decreasing relation.

	Dependency on geom. param.		
Model param.	$W_{\mathbf{Rx}}$	$S_{\mathbf{Rx}}$	$N_{\mathbf{Rx}}$
V_{emf}	↘	↘	N_{Rx}
L_{Rx}	$\log W_{\text{Rx}}$	-	N_{Rx}^2
R_{Rx}	W_{Rx}^{-1}	-	$N_{\text{Rx}}, N_{\text{Rx}}^2$
R_{sub}	↘	↘	↘
C_{sub}	↗	↗	↗
C_{turn}	-	S_{Rx}^{-1}	↗

decreasing the inter-turn capacitance roughly inversely proportional to S_{Rx}. N_{Rx} increases the induced emf voltage in the coil roughly linearly [12], while the coil inductance increases roughly proportionally to the square of N_{Rx} [13]. We say roughly because the diameter of each turn is not uniform for a printed spiral coil, nor is the coil circular and hence the assumption of an ideal coil is an approximation. Because the inner turns will attain smaller diameters if either W_{Rx} or S_{Rx} are increase, V_{emf} will decrease slightly for such a case. Additionally, increasing N_{Rx} adds a roughly linear term to the ESR because the coil gets longer roughly proportionally to the number of turns. Furthermore, because the inductive coupling to substrate or substrate shield increases with the square of N_{Rx} [14], another term, N_{Rx}^2, is added to R_{Rx}.

It is assumed that the optimised coil geometries will have values for the turn separation of the Rx coil, S_{Rx}, that makes the effect of the inter-turn capacitance on the power delivered to the load negligible and thus, this effect is ignored henceforth. Furthermore, we do not attempt to estimate values for C_{sub} and R_{sub} due to the complexity of such a task, but merely discuss the limitations the effect as a whole imposes on the coil design. Thus, for calculations, we assume that the effects of C_{sub} and R_{sub} are represented in $\mathbf{V_{emf}}(\mathrm{j}\omega)$, L_{Rx} and R_{Rx}.

3.2 Maximum Load Resistance

As explained in Section 2.2, the on-chip matching network consists of a single shunt capacitor. A series capacitor would cancel out the inductive reactance, while a shunt capacitor would also transform the resistive part of a load impedance to a smaller one. For low-power operation, the load resistance is assumed to be larger than the magnitude of the source impedance given by the ESR of the Rx coil in series with the coil reactance. Thus, in order to bring the load resistance as closely as possible to the magnitude of the source impedance, the matching network consist of a shunt capacitor, as illustrated in Figure 4.

To simplify the analysis and without loss of generality, the average equivalent load resistance, $R_{\text{L,avg}}$, is used for calculations.

The power, P_{L}, delivered to the average equivalent load, $R_{\mathrm{L,avg}}$ is given by

$$P_{\mathrm{L}} = \left| \mathbf{V_{emf}}(\mathrm{j}\omega) \frac{Z_{\mathrm{eq}}}{Z_{\mathrm{eq}} + R_{\mathrm{Rx}} + \mathrm{j}\omega L_{\mathrm{Rx}}} \right|^2 \Big/ R_{\mathrm{L,avg}} \ , \tag{1}$$

where $\mathbf{V_{emf}}(\mathrm{j}\omega)$ is the input voltage phasor generated in the Rx coil by the signal transmitted from the Tx coil, ω is the angular operating frequency and Z_{eq} is the equivalent impedance from the parallel connection formed by $C_{\mathrm{m,Rx}}$ and $R_{\mathrm{L,avg}}$, given by

$$Z_{\mathrm{eq}} = \frac{R_{\mathrm{L,avg}}/\mathrm{j}\omega C_{\mathrm{m,Rx}}}{R_{\mathrm{L,avg}} + 1/\mathrm{j}\omega C_{\mathrm{m,Rx}}} = \frac{R_{\mathrm{L,avg}} - \mathrm{j}\omega C_{\mathrm{m,Rx}} R_{\mathrm{L,avg}}^2}{\omega^2 C_{\mathrm{m,Rx}}^2 R_{\mathrm{L,avg}}^2 + 1}. \tag{2}$$

Substituting Eq. (2) into Eq. (1), it can be shown that P_{L} can be expressed as

$$P_{\mathrm{L}} = V_{\mathrm{emf}}^2 \frac{R_{\mathrm{L,avg}}}{R_{\mathrm{L,avg}}^2 \left[1 + \omega^2 C_{\mathrm{m,Rx}}^2 \left(R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2\right) - 2\omega L_{\mathrm{Rx}} \omega C_{\mathrm{m,Rx}}\right] + R_{\mathrm{Rx}}^2 + 2R_{\mathrm{L,avg}} R_{\mathrm{Rx}} + \omega^2 L^2}, \tag{3}$$

where V_{emf} is the amplitude of the input voltage phasor, $\mathbf{V_{emf}}(\mathrm{j}\omega)$.

It can be seen from Eq. (3) that for a fixed on-chip coil design (constant V_{emf}, $R_{\mathrm{L,avg}}$, R_{Rx}, L_{Rx} and ω), in order to maximise P_{L}, the expression

$$f(\omega C_{\mathrm{m,Rx}}) = \omega^2 C_{\mathrm{m,Rx}}^2 \left(R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2\right) - 2\omega L_{\mathrm{Rx}} \omega C_{\mathrm{m,Rx}} \tag{4}$$

should be minimised. Because

$$\frac{\mathrm{d}^2 f(\omega C_{\mathrm{m,Rx}})}{\mathrm{d}(\omega C_{\mathrm{m,Rx}})^2} = 2\left(R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2\right) \tag{5}$$

is positive,

$$\frac{\mathrm{d} f(\omega C_{\mathrm{m,Rx}})}{\mathrm{d}(\omega C_{\mathrm{m,Rx}})} = 2\omega C_{\mathrm{m,Rx}} \left(R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2\right) - 2\omega L_{\mathrm{Rx}} = 0 \tag{6}$$

yields a local minimum point for $\omega C_{\mathrm{m,Rx}}$; namely

$$\omega C_{\mathrm{m,Rx}} = \frac{\omega L_{\mathrm{Rx}}}{R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2}. \tag{7}$$

Inserting Eq. (7) into Eq. (3) yields

$$P_{\mathrm{L,max}} = V_{\mathrm{emf}}^2 \frac{R_{\mathrm{L,avg}}}{\gamma R_{\mathrm{L,avg}}^2 + 2R_{\mathrm{L,avg}} R_{\mathrm{Rx}} + R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2}, \tag{8}$$

where

$$\gamma = 1 - \frac{\omega^2 L_{\mathrm{Rx}}^2}{R_{\mathrm{Rx}}^2 + \omega^2 L_{\mathrm{Rx}}^2} = \frac{1}{Q_{\mathrm{Rx}}^2 + 1}, \tag{9}$$

where $Q_{\mathrm{Rx}} = \omega L_{\mathrm{Rx}}/R_{\mathrm{Rx}}$ is the Q factor of the Rx coil. Assuming a reasonably high Q_{Rx}, $\omega^2 L_{\mathrm{Rx}}^2 \gg R_{\mathrm{Rx}}^2$, and Eq. (8) reduces to

$$P_{\mathrm{L,max}} \approx \frac{V_{\mathrm{emf}}^2}{\gamma R_{\mathrm{L,avg}} + 2R_{\mathrm{Rx}} + \omega^2 L_{\mathrm{Rx}}^2 / R_{\mathrm{L,avg}}}. \tag{10}$$

Table 2: Conditions for the different regions of operation for a coupled PCB-IC coil system with a single on-chip shunt capacitor as matching network at the IC side.

Region	**Condition**
High-power	$\gamma R_{\mathrm{L,avg}}$ significant in the denominator of Eq. (10)
Medium-power	$\gamma R_{\mathrm{L,avg}}$ insignificant in the denominator of Eq. (10) and it is possible to increase η by increasing N_{Rx}
Low-power	$\gamma R_{\mathrm{L,avg}}$ insignificant in the denominator of Eq. (10), but it is not possible to increase η by increasing N_{Rx}

$P_{\mathrm{L,max}}$ in Eqs. (8) and (10) represent the maximum obtainable power for a fixed on-chip coil design assuming an ideal matching capacitor, $C_{\mathrm{m,Rx}}$. A method for manufacturing trimmable, high Q factor IC capacitors which can be utilised in order to approximate such a capacitor has been proposed in [15]. As can be seen from Eq. (9), γ will decrease with increasing Q factor. Thus for high Q factors, $R_{\mathrm{L,avg}}$ will be less significant for $P_{\mathrm{L,max}}$ and in turn for the power transfer efficiency, $\eta = P_{\mathrm{L,max}}/P_{\mathrm{S}}$. Based on observed IC coil Q factors from this and previous works [1,2], for optimised coils, γ typically attains values of around 0.6-10 %.

In the following, we will show that a coupled PCB-IC coil system of this paper operates in three different regions of operation characterised by the power consumption at a load. We denote these regions the *high-power*, *medium-power* and *low-power* regions of operation. The conditions for these regions are listed in Table 2, and the remainder of this section is devoted to analysing their characteristics and conditions.

As noted in Table 1, the induced voltage amplitude, V_{emf}, is proportional to the number of turns in the receiver coil, N_{Rx}, while the inductance, L_{Rx}, is proportional to N_{Rx}^2. Thus, Eq. (10) shows that increasing N_{Rx} beyond the point where $\omega^2 L^2/R_{\mathrm{L,avg}}$ starts to become dominant will reduce the maximum power delivered to the load, $P_{\mathrm{L,max}}$. We say that the system transitions from operating in the high-power region to the medium-power region at this point. Due to the previous reasoning, it can thus be assumed that for an optimal coil design, $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}} \ll \gamma R_{\mathrm{L,avg}} + 2R_{\mathrm{L,avg}}$ and Eq. (10) reduces to

$$P_{\mathrm{L,max}} \approx \frac{V_{\mathrm{emf}}^2}{\gamma R_{\mathrm{L,avg}} + 2R_{\mathrm{Rx}}}. \tag{11}$$

However, it should be noted that this assumption ignores the fact that the number of turns must be a non-zero integer. The assumption may thus be false for designs with few turns for which the impedance, $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$, (the values of which are quantised for a constant $R_{\mathrm{L,avg}}$ due to the quantised nature of N_{Rx}) may be excessively small compared to $2R_{\mathrm{Rx}}$. Thus for some designs, a unit increment in N_{Rx} would result in an increase in $P_{\mathrm{L,max}}$ because the benefit of a higher V_{emf} would be bigger than the drawback of a higher $\omega^2 L_{\mathrm{Rx}}^2$. Thus for medium-power operation, the approximation given in Eq. (11) is valid, but for for high-power operation, it may be invalid and we should resort to using Eq. (10).

Because $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$ will dominate the denominator of Eq. (10) only for small values of $R_{\mathrm{L,avg}}$, it is only relevant for high-power operation, which is not the focus of this

work. However, it should nonetheless be noted that because $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$ is significantly more detrimental for $P_{\mathrm{L,max}}$ than is $\gamma R_{\mathrm{L,avg}}$ in this region of operation, it would be more beneficial to employ a series capacitor matching network which would fully cancel the coil reactance. The maximum power consumption for series matching network would then be given by Eq. (8), but with $\gamma = 1$ and $\omega L_{\mathrm{Rx}} = 0$, that is

$$P_{\mathrm{L,max,series}} = V_{\mathrm{emf}}^2 \frac{R_{\mathrm{L,avg}}}{R_{\mathrm{L,avg}}^2 + 2R_{\mathrm{L,avg}}R_{\mathrm{Rx}} + R_{\mathrm{Rx}}^2}. \tag{12}$$

The drawback here is that the $R_{\mathrm{L,avg}}^2$ term in the denominator of Eq. (8) is no longer reduced by a factor γ and thus, if $R_{\mathrm{L,avg}}^2$ is dominant, the power delivered to the load will be reduced, again illustrating that a series-capacitor topology is sub-optimal for medium- and low-power operation.

For medium-power operation, $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$ will no longer be dominant in the denominator of Eq. (11). Thus, in this region, the more $R_{\mathrm{L,avg}}$ is increased, the more N_{Rx} can grow without being detrimental for $P_{\mathrm{L,max}}$. From Eq. (11) and Table 1, it can be seen that an increase in N_{Rx} will generate a quadratic increase in $P_{\mathrm{L,max}}$ due to the resulting increase in V_{emf}. However, R_{Rx} will increase linearly, which is detrimental for $P_{\mathrm{L,max}}$, but is detrimental at a smaller extent than the increase in V_{emf} is beneficial for $P_{\mathrm{L,max}}$. However, a linear increase in R_{Rx} will also result in a quadratic increase in the Q_{Rx}^2 term in the denominator of γ in Eq. (9). Nevertheless, because of the typically low Q factors of on-chip coils, the unity term in the denominator of Eq. (9) may be significant, resulting in an overall reduction in γ that is less than quadratic and which can thus be less detrimental for P_{L} than the quadratic increase in V_{emf}. Therefore, W_{Rx} can decrease slightly, in turn increasing V_{emf} slightly because of the increased radii of the inner turns, without the resulting increase in R_{Rx} consequentially resulting in that $2R_{\mathrm{Rx}}$ becomes the dominant term in the denominator of Eq. (11) and without scaling up γ by more than the by how much V_{emf}^2 was scaled. A consequence of this behaviour is that, when the power transfer efficiency, $\eta = P_{\mathrm{L,max}}/P_{\mathrm{L}}$, decreases due to increasing $R_{\mathrm{L,avg}}$, the power delivered to the load, $P_{\mathrm{L,max}}$, can still increase (for the same transmitted power, P_{S}) due to the boosts in V_{emf} resulting from an increased number of turns and increasing diameters of the inner turns due to a smaller trace width.

However, there is a limit for the load for when increasing the number of turns, N_{Rx}, will stop being beneficial for $P_{\mathrm{L,max}}$. Because of the diminishing returns in the increase in V_{emf} due to the increasingly smaller radii of the inner turns when a turn is added and the increasingly limiting effects of the substrate when the fill factor of the coil is increased, beyond this limit, which we denote $R_{\mathrm{L,cutoff}}$, an increase in N_{Rx} will instead be detrimental for $P_{\mathrm{L,max}}$. For values for $R_{\mathrm{L,avg}} > R_{\mathrm{L,cutoff}}$, the strategy of increasing $R_{\mathrm{L,avg}}$ in an attempt to move towards lower power operation becomes ineffective because $P_{\mathrm{L,max}}$, and in turn η, are reduced with the same factor as the load current (which is given by $V_{\mathrm{L}}/R_{\mathrm{L,avg}}$). The implication is that, beyond this point, reducing the load current does not significantly increase the available supply voltage, V_{L}, for a given V_{emf}.

When N_{Rx} no longer can be increased, the benefits by a decrease in W_{Rx} seen for medium-power operation will no longer apply and the coil geometry will thus not vary

much in the region of low-power operation. Consequentially, in the low-power region, $2R_{\mathrm{Rx}}$ will no longer increase and $\gamma R_{\mathrm{L,avg}}$ will be dominant in the denominator of Eq. (11). Therefore, $\gamma R_{\mathrm{L}} \gg 2R_{\mathrm{Rx}}$ and Eq. (11) can be approximated by

$$P_{\mathrm{L,max}} \approx \frac{V_{\mathrm{emf}}^2}{\gamma R_{\mathrm{L,avg}}}. \tag{13}$$

Because of the coil geometry invariance in the low-power region of operation, a viable strategy for finding $R_{\mathrm{L,cutoff}}$ may be to determine the impedance of an optimised coil geometry for a high $R_{\mathrm{L,avg}}$ (well into the low-power region) and use the result to calculate values for the impedances $\gamma R_{\mathrm{L,avg}}$ and $2R_{\mathrm{Rx}}$. At the transition from medium-power to low-power operation, $2R_{\mathrm{Rx}}$ will stop being significant, and thus at this point, it can be assumed that $2R_{\mathrm{Rx}}$ will be only slightly smaller than $\gamma R_{\mathrm{L,avg}}$. We denote the fraction that relates $\gamma R_{\mathrm{L,avg}}$ to $2R_{\mathrm{Rx}}$ as β. Thus, for low power operation:

$$2R_{\mathrm{Rx}} = \beta\gamma R_{\mathrm{L,avg}}. \tag{14}$$

The cut-off point, $R_{\mathrm{L,cutoff}}$ can then be found by substituting $R_{\mathrm{L,avg}} = R_{\mathrm{L,cutoff}}$ into Eq. (14) and solving for $R_{\mathrm{L,cutoff}}$. $R_{\mathrm{L,cutoff}}$ is then given by

$$R_{\mathrm{L,cutoff}} = \frac{2R_{\mathrm{Rx}}}{\beta\gamma} = 2R_{\mathrm{Rx}}\left(Q_{\mathrm{Rx}}^2 + 1\right). \tag{15}$$

Towards the end of Section 4, we will empirically determine a suitable value for β.

4 Coil Geomery Optimisation for Varying Load

A gradient ascent algorithm was used in conjunction with the electromagnetic simulator FEKO [16] in order to optimise the coil geometries for high power transfer efficiency. The algorithm is the same as from our earlier work [4], based on an algorithm originally presented by Zargham and Gulak [1]. Pseudo-code for the algorithm is repeated for reference in this work in Table 3.

For the electromagnetic simulations, a IC chip was modelled in direct contact with a power semiconductor inside a module as shown in Figure 1. An extended version of the schematic including material information is shown in Figure 6, while permittivities and conductivities for the materials are listed in Table 4. In order to shorten simulation times, the model was simulated in 2.5-dimensional (2.5D) mode, where the layers of the different materials are modelled as infinite slabs in the horizontal direction. A 350 nm process with 4 metal layers was used. Out of these layers, the top 2 layers, metal 3 and metal 4 were used for the coil, stitched together with vias at the corners, realising a parallel connection. The bottom metal layer, metal 1, was used to shield the on-chip coil from the conductive substrate [1]. The shield consist of a chopped-up coil laid out directly underneath the Rx coil.

The coil geometries were optimised in order to maximise the power transfer efficiency, η, for different average equivalent load resistances, $R_{\mathrm{L,avg}}$, a coil separation of $D = 10\,\mathrm{mm}$

Table 3: Power transfer effiency optimisation algorithm for coil geometries. Originally published in [4] and based on [1].

step 1: initialisation

$N_{\mathrm{Tx}} := 1$

$W_{\mathrm{Tx}} :=$ minimum allowed PCB trace width

$S_{\mathrm{Tx}} :=$ minimum allowed PCB trace separation

$d_{\mathrm{Tx}} := D \cdot \sqrt{2\left(1+\sqrt{5}\right)}$

$N_{\mathrm{Rx}} := 1$

$W_{\mathrm{Rx}} :=$ minimum allowed chip trace width

$S_{\mathrm{Rx}} :=$ minimum allowed chip trace separation

$d_{\mathrm{Rx}} :=$ chip die size

step 2: Tx coil quality factor optimisation

for $1 \leq N_{\mathrm{Tx}} \leq 12$:
  gradient ascent algorithm:
    search: N_{Tx}, W_{Tx}, S_{Tx}
    maximise: Q_{Tx}
update: N_{Tx}, W_{Tx}, S_{Tx} for maximum Q_{Tx}

step 3: Rx coil quality factor optimisation

for $1 \leq N_{\mathrm{Rx}} \leq 12$:
  gradient ascent algorithm:
    search: N_{Rx}, W_{Rx}, S_{Rx}
    maximise: Q_{Rx}
update: N_{Rx}, W_{Rx}, S_{Rx} for maximum Q_{Rx}

step 4: Tx coil-based power transfer efficiency optimisation

for $1 \leq N_{\mathrm{Tx}} \leq 12$:
  gradient ascent algorithm:
    search: N_{Tx}, W_{Tx}, S_{Tx}, d_{Tx}
    maximise: η
update: N_{Tx}, W_{Tx}, S_{Tx}, d_{Tx} for maximum η

step 5: Rx coil-based power transfer efficiency optimisation

for $1 \leq N_{\mathrm{Rx}} \leq 12$:
  gradient ascent algorithm:
    search: N_{Rx}, W_{Rx}, S_{Rx}
    maximise: η
update: N_{Rx}, W_{Rx}, S_{Rx} for maximum η

step 6: stop condition

if η improved since step 4:
  go to step 4
else:
  stop

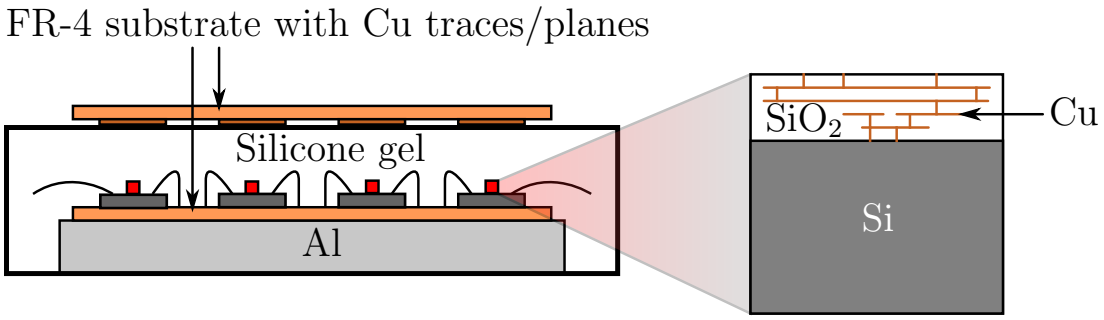

Figure 6: Material information for the monitoring system shown in Figure 1.

Table 4: Material properties for the materials used in this work.

Material	**Rel. permittivity**	**Conductivity** [MS/m]
Silicon substrate	11.7	*not available**
Silicon dioxide	3.9	∼0
Silicone gel	2.1	∼0
FR-4	4.4	∼0
Copper	1	59.6

*Value known and used for simulations, but can not be published due to non-disclosure agreement.

and an outer diameter for the Rx coil of $d_{\mathrm{Rx}} = 2\,\mathrm{mm}$. In order to assess which is the most favourable frequency, simulations were first run in order to optimise η for $R_{\mathrm{L,avg}} = 100\,\mathrm{k\Omega}$. The frequency bands 44.66, 169.4, 433.0 and 868.0 MHz were examined. These are industrial, scientific and medical (ISM) bands or other frequency bands recommended by the Swedish post and telecommunications authority [17]. Out of these, 169.4 MHz yielded the highest power transfer efficiency at $\eta = -45.5\,\mathrm{dB}$, and so, the remainder of the simulations presented in this section were carried out at this frequency[1].

To visualise the characteristics of the best values of power transfer efficiency, the coil geometries were optimised during two months to maximise η for various values of $R_{\mathrm{L,avg}}$. The best values found by the optimiser are shown in Figs. 7 and 8, where the power transfer efficiency and its corresponding Rx coil geometry, respectively, are plotted against $R_{\mathrm{L,avg}}$. Also shown are the high-power, medium-power and low-power regions of operation as described in Section 3.2. From Figure 7 it can be seen that the maximum power transfer efficiency occurs in the high-power region, around $R_{\mathrm{L,avg}} = 180\,\Omega$. We comment on the Rx coil dimensions in relation to power transfer efficiency later in this

[1]We should note that this frequency differs from the one obtained in our earlier work; 433 MHz [4]. The reason for this is a previous error in the model which placed the substrate farther apart from the copper traces than it should be, resulting in underestimated substrate effects. This error has since been corrected and the corrected version is used for the simulations in this work. As a result of this error, the results obtained in our previous work also overestimates the power transfer efficiency. The power transfer efficiencies shown in this work are verified against measurements and are thus believed to be correct.

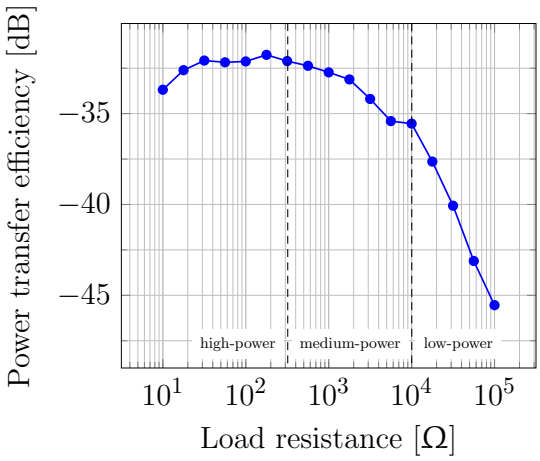

Figure 7: Power transfer efficiency of coils optimised for different average equivalent load resistances.

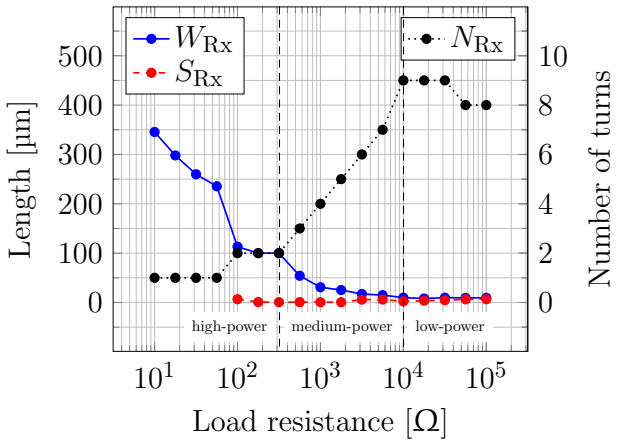

Figure 8: Optimised geometry of the Rx coil plotted as a function of average equivalent load resistance. The trace separation is not defined for coil geometries with only a single turn, which is why values are missing for S_{Rx} for load resistances smaller than $100\,\Omega$.

section. The optimisation algorithm yielded roughly the same geometry for the Tx coil for all the examined average equivalent load resistances and thus we present its geometry and Q factor for the arbitrarily chosen value of $R_{\mathrm{L,avg}} = 10\,\mathrm{k}\Omega$ in table form in Table 5. The lack of variation is expected due of the weak coupling between the coils which results in that the effect of the loading of the Rx side is not very significant for the Tx coil.

In the following reasoning, we assume that the optimiser has found near-optimal coil geometries. Figure 9 shows plots of the impedances of the terms in the denominator of Eq. (10) as a function of load resistance. Looking at both the figure and the equation, it can be seen that $\omega^2 L_{\mathrm{Rx}}^2 / R_{\mathrm{L,avg}}$ stops being significant for $P_{\mathrm{L,max}}$ at around $R_{\mathrm{L,avg}} = 320\,\Omega$. Looking back at Figure 7 it can be seen that it is around this point that η starts to fall off, and at around $R_{\mathrm{L,avg}} = 10\,\mathrm{k}\Omega$, the maximum decline of 10 dB per decade increase in

Table 5: Optimised coil geometry and Q factor for the Tx coil at a load resistance of 10 kΩ.

Parameter		**Value**
Trace width,	W_{Tx}	3.0 mm
Trace seperation,	S_{Tx}	1.5 mm
Outer dimension,	d_{Tx}	25.4 mm
No. of turns,	N_{Tx}	2
Q factor,	Q_{Tx}	139.4

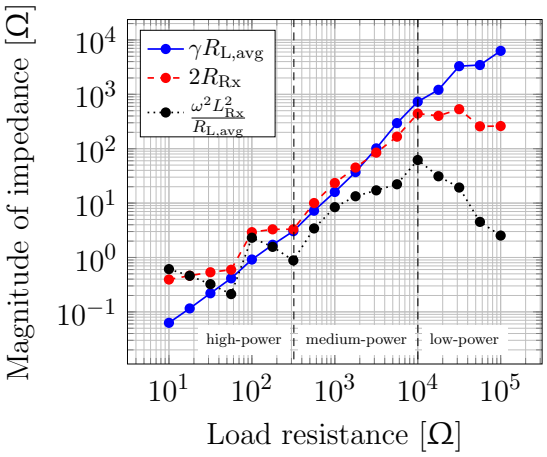

Figure 9: Magnitude of the impedance terms in the denominator of Eq. (10) for the Rx coil optimised at different average equivalent load resistances.

$R_{\mathrm{L,avg}}$ is reached. As argued in Section 3.2, it is beyond this point that, for a constant load voltage, there is no reduction in the required transmitter power, P_{S}, even if an attempt to reduce it is made by increasing $R_{\mathrm{L,avg}}$ because the current consumption—and hence the power delivered to the load, P_{L}—decrease at the same rate as the does power transfer efficiency, η. This phenomenon can be seen in Figure 10. Here, both P_{L} and η are plotted as functions of load resistance, and the figure also plots the power consumption of the transmitting coil, P_{S}, required in order to realise a root-mean-square (rms) load voltage, V_{L}, of 1 V. The purpose of presenting plots for constant V_{L} is to uncover the behaviour of P_{L} when the current consumption is solely dependent on load resistance. The figure shows that the required transmitting power decreases up to the point where the plotted slopes of P_{L} and η become equal, at which point P_{S} starts to level off, asymptotically reaching a constant value of around 25 dBm at around $R_{\mathrm{L,avg}} = 10\,\mathrm{k}\Omega$.

It is interesting to analyse Figs. 8, 9 and 10 further. It can be seen that in the region of high-power operation, where $R_{\mathrm{L,avg}} < 320\,\Omega$, either $2R_{\mathrm{Rx}}$ or $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$ is dominant and L_{Rx} must be kept low in order to not be detrimental for P_{L}. Because of the strong dependence of L_{Rx} on N_{Rx}, N_{Rx} will be kept low in this region as can be seen from Figure 8. An exception is $R_{\mathrm{L,avg}} = 100\,\Omega$, where it turns out that increasing N_{Rx} by one turn was more beneficial for P_{L} due to the increase in V_{emf} than it was detrimental due to the increase in L_{Rx}. However, when $\omega^2 L_{\mathrm{Rx}}^2/R_{\mathrm{L,avg}}$ is surpassed by both $\gamma R_{\mathrm{L,avg}}$

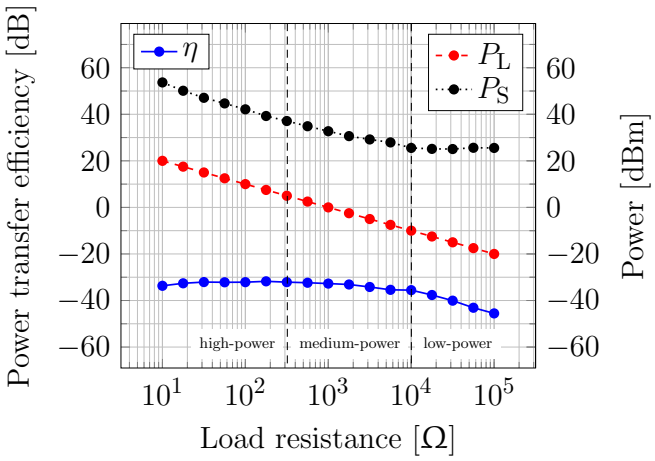

Figure 10: Power transfer efficiency, η, transmitted power, P_S, and consumed power, P_L, for coils optimised for different Equivalent average load resistances. P_S is the power delivered to the transmitting coil required in order to maintain an rms voltage of 1 V *over the load, while P_L is the power consumed at the load.*

and $2R_{\mathrm{Rx}}$, L_{Rx} can grow without a reduction in P_{L} while the system is transitioning into the medium-power region. A consequence is that N_{Rx} starts growing steadily at around $R_{\mathrm{L,avg}} = 320\,\Omega$ after which $\omega^2 L_{\mathrm{Rx}}^2 / R_{\mathrm{L,avg}}$ never again becomes dominant. N_{Rx} grows until it reaches a maximum of $N_{\mathrm{Rx}} = 8$ or 9 where additional turns will be detrimental to P_{L}—due to the diminishing returns in inductance for additional turns and to stronger substrate effects—more than it will benefit P_{L} due to the increase in V_{emf}.

Figure 11 shows the Q factors resulting from optimising the Rx coil for different average equivalent load resistances, $R_{\mathrm{L,avg}}$. The figure shows that while the Q factor is relatively high for low $R_{\mathrm{L,avg}}$, it rapidly starts dropping off when the system transitions into the medium-power region of operation and eventually reaches a minimum of $Q_{\mathrm{Rx}} = 3$ to 4 when the system reaches the low-power region. This behaviour is expected because the number of turns, N_{Rx} is fairly constant in the high- and low-power regions, while steadily increasing in the medium-power region. A high number of turns will decrease Q_{Rx} because the trace width, W_{Rx}, will decrease to accommodate the additional turns. On top of this, because the inner turns have smaller diameters compared to the outer one, the increase in inductance will diminish as N_{Rx} grows larger, further decreasing the Q factor.

Figure 8 shows that S_{Rx} remains fairly constant throughout the entire load resistance range. An explanation for this could be that the value S_{Rx} attains simply makes the inter-turn capacitance, C_{turn}, negligible for the frequency in question.

Furthermore, in order to estimate a suitable value for β in Eq. (15), Eq. (14) is solved for β and values are for $\gamma R_{\mathrm{L,avg}}$ and $2R_{\mathrm{Rx}}$ are obtained from Figure 9 at the observed transition to the low-power region, at $R_{\mathrm{L,avg}} = 10\,\mathrm{k}\Omega$. By this procedure, a value of $\beta = 0.6$ is obtained. Using this value for β, in order to test the validity of the theory on how to estimate $R_{\mathrm{L,cutoff}}$, values for $\gamma R_{\mathrm{L,avg}}$ and $2R_{\mathrm{Rx}}$ are taken from Figure 9 at $R_{\mathrm{L,avg}} = 100\,\mathrm{k}\Omega$ and inserted into Eq. (15). The result is $R_{\mathrm{L,cutoff}} = 6.8\,\mathrm{k}\Omega$, reasonably

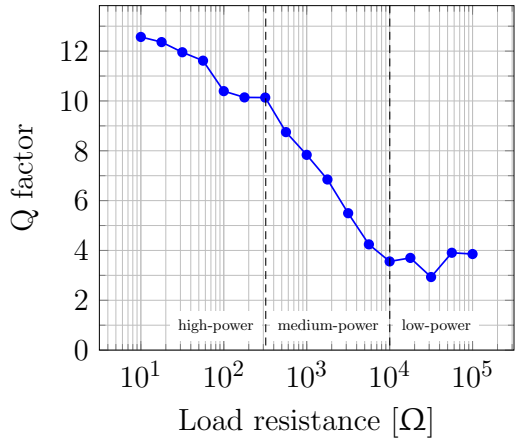

Figure 11: Q factor of the Rx coil optimised at different load resistances.

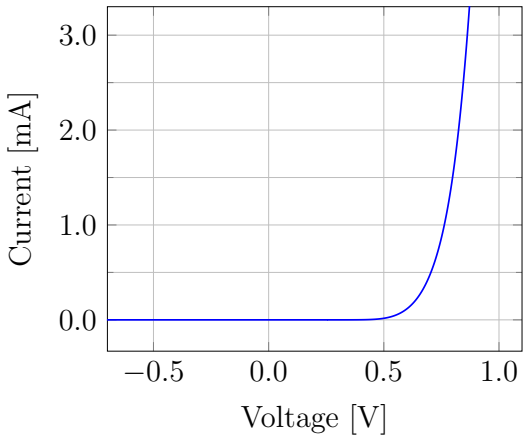

Figure 12: Current–voltage characterisation of the MOSFET diode, M_D.

close to the observed cut-off point at $R_{\mathrm{L,cutoff}} = 10\,\mathrm{k\Omega}$.

5 Measurements

In this section we present measurements used to confirm the validity of the simulations presented in the previous section.

5.1 MOSFET Diode Characterisation

In order to accurately estimate the power transfer efficiency, η, of the system described in Section 2, the MOSFET diode, M_{D}, was characterised. This was done by sweeping the DC current of a Keithley 2450 source meter while monitoring the resulting voltage. The result is presented in Figure 12. The figure reveals a forward voltage, V_{D}, of between 500 and 750 mV for a forward current between 10 and 1000 µA.

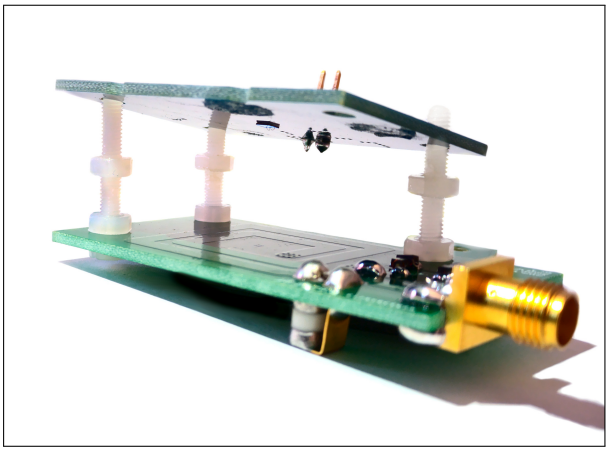

Figure 13: PCB with IC with on-chip coil on the bottom side mounted 10 mm *above PCB with Tx coil.*

5.2 Power Transfer Efficiency Characterisation for Varying Load Resistance

An experimental set-up was arranged according to Figure 3 with a matched PCB coil driven by a power amplifier. An IC containing an on-chip coil, a shunt capacitor as matching network and a rectifier was manufactured in a 350 nm CMOS process and is modelled on the optimised design presented in our previous work, [4]. This is a 5-turn coil with a trace width of 35 µm, a trace separation of 6.0 µm and an outer diameter of 2.0 mm. Although that design turned out to be sub-optimal due to a previous error in the simulation model as detailed in Section 4, we use that design in this work in order to verify our now corrected simulation model. The IC was glued to a PCB mounted at 10 mm from the Tx PCB as shown in the picture of Figure 13. In order to emulate the situation in a monitoring system for power semiconductor modules where the sensors would be mounted some distance above a ground plane, the Rx PCB included a buried ground plane at a depth of 1.6 mm. This plane was also included in all simulations presented in this paper. To reduce the amount of induced current at sensitive nodes, the length of bond wires were kept to a minimum and the circuit goes directly down through vias at the bond wire pads to the bottom layer of the PCB, where the load resistor, R_{L}, and voltage follower were placed as closely as possible to the vias.

The diode characterisation described in Section 4 was used to estimate the power transfer efficiency, $\eta = P_{\mathrm{L}}/P_{\mathrm{S}}$ based on observed voltages, V_{L}, at R_{L} for different values of load resistance. For each load resistance point, the power was increased until a V_{L} of 300 mV was obtained. The load resistances used ranged from 560 Ω to 100 kΩ. Due to the excessive power requirements, it was not possible to drive the PCB coil at lower resistances. Therefore the power transfer efficiency characterisation was repeated for a two-turn, wire-wound air coil used as Tx coil and placed directly around the Rx chip as shown in the picture of in Figure 14. Because of the closer proximity and higher Q factor of the wire coil, a higher efficiency was achieved and it was possible to perform the

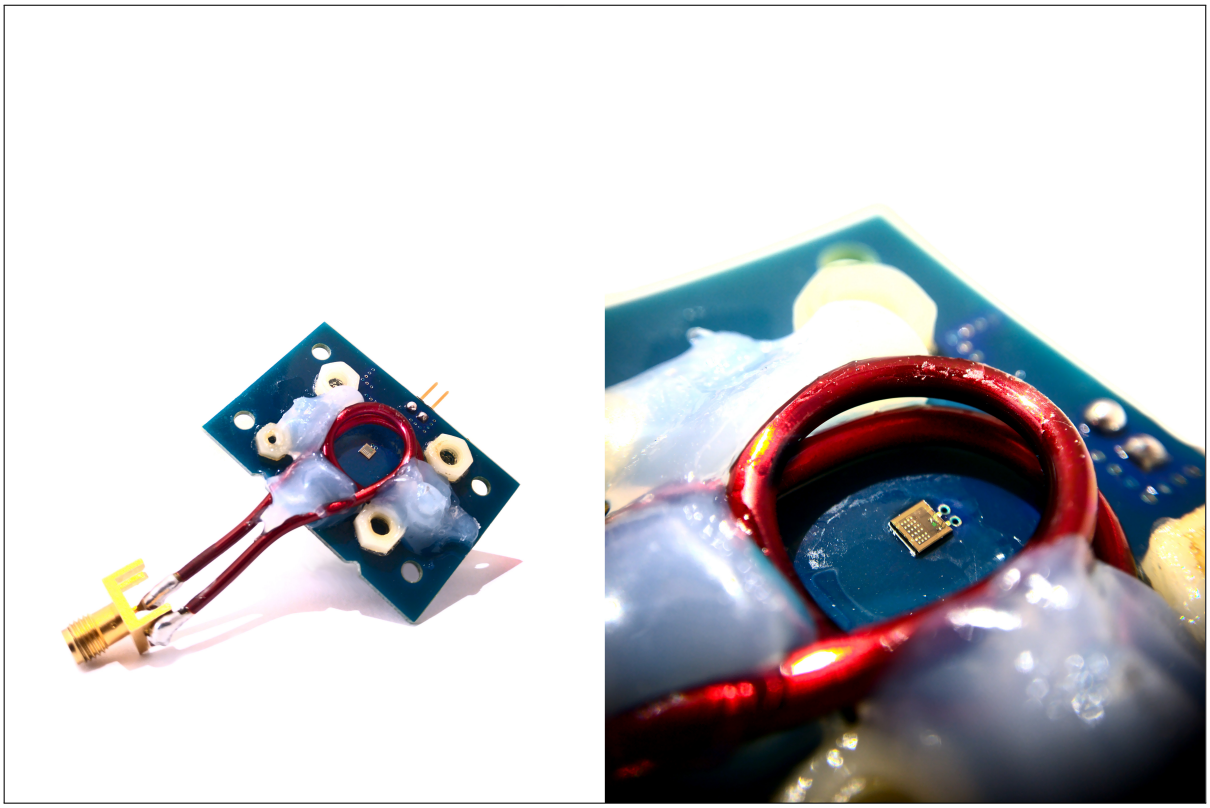

Figure 14: Wire coil glued around IC with on-chip coil.

measurements for load resistances down to $R_{\mathrm{L,avg}} = 56\,\Omega$. Because of the weak coupling between Tx and Rx coils, as is also the case for the PCB coil variant of this set-up, the resistance at the Rx side is insignificant for the Tx coil. Therefore, the power transfer efficiencies for the two cases (PCB coil and wire coil) should differ by a constant factor over the full resistance range. For the performed measurements, this factor was estimated to approximately 6 dB. Figure 15 shows a plot of the power transfer efficiency from both types of measurement as a function of load resistance along with circuit simulations based on coil parameters given by electromagnetic simulations. These simulations use the same layer structure and material properties as the simulations presented in Section 4, except that air was used in place of the silicone gel. The power transfer efficiency for the wire coil has been shifted downwards by 6 dB and thus shows the expected behaviour of the PCB coil to be seen had measurements been done for lower load resistances.

Comparing the measurements with simulated values, Figure 15 shows close agreement in general behaviour of the two graphs. However, the measured values differ by an approximately constant value between 5 and 12 dB. This discrepancy can have several explanations:

One possible explanation could be that because the Tx coil is very low impedance, the ESR of the matching components may be significant because they are comparable in size to the coil impedance. ESR values of $R_{\mathrm{L,m}} = 53\,\mathrm{m}\Omega$ and $R_{\mathrm{C,m}} = 35\,\mathrm{m}\Omega$ for the

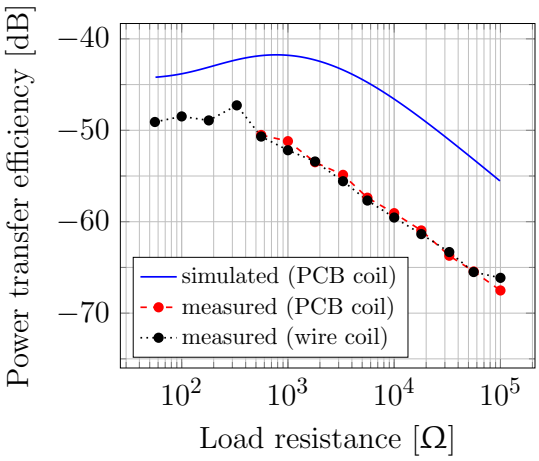

Figure 15: Simulated and measured values of the power transfer efficiency in an inductive link between two coils for various load resistances. The measurements for the wire coil have been shifted has been shifted downwards by 6 dB *to facilitate comparison with the PCB coil measurements.*

matching shunt inductor, $L_{\mathrm{m,Tx}}$, and series capacitor, $C_{\mathrm{m,Tx}}$, were obtained obtained from data sheets. These are comparable to the ESR of the Tx coil of $R_{\mathrm{Tx}} = 573\,\mathrm{m\Omega}$ and are thus likely significant, but circuit simulations show that they are unlikely to be the full explanation for the discrepancy in power transfer efficiency.

Another possibility could be that the DC characterisation of the MOSFET diode is not valid for the high-frequency case. However, no unexpected power consumption in the diode is visible in circuit simulations. It is however possible that the simulator omits effects such as those from the parasitic body diode which would exhibit a significant turn-off time due to the reverse-recovery effect [18] than a pure MOSFET diode and thus result in an increased reverse-leakage current during the negative half-cycles of the transmitted signal. To examine whether this was the case, the coils were immersed in liquid nitrogen in order to cool them down to −196 °C. Because the reverse-recovery time in p-n junctions is proportional to absolute temperature [18], if p-n junction leakage is in fact a problem, it should be heavily mitigated by the lower temperature. However, the power transfer efficiency increased by merely 5 dB for the nitrogen-cooled coils, which is less than what is expected due to decreased resistance in the copper traces of the coils at the reduced temperature, which amounts to approximately 7 dB. Thus, the possibility of parasitic body diode turn-on being the main contributing factor is ruled out.

Another source of error could be induced currents in bond wires or in PCB tracks at the Rx side interfering with the rectifier. Even though care was taken to reduce the loop area of the critical part of the circuit, parasitic induced currents could be comparable in magnitude to those induced in the on-chip coil because of the small total loop area of the coil. However, it is difficult to quantify the magnitude of this effect or determine whether it is significant.

It is also possible that the accuracy of the electromagnetic model is responsible for

the discrepancy. The dielectric materials in the model are modelled as infinite layers in order to speed up the simulations. Had a full 3-dimensional (3D) model been used, it is possible that the accuracy could have been increased.

Furthermore, the manufacturing tolerances for the thicknesses of the layers in the manufactured ICs are large, thus it is possible that parasitic elements such as e.g. substrate capacitance are more prominent than the simulation model shows.

In conclusion, we have identified some possible sources of errors in an attempt to explain the discrepancy between simulation models and measurement results. While it is difficult to say exactly which sources are most significant it is likely that the discrepancy does not have a single cause, but is rather a combination of multiple sources of error. However, we note again that the graphs exhibit a good matching in overall shape.

6 Conclusion

We have shown theoretically that for the low-power operation of on-chip coils with shunt capacitors as matching networks, there is a limit for where it is inefficient to further decrease the load in an attempt to reduce the transmitted power. For the 350 nm CMOS process used, this limit appears to lie around 10 kΩ. This means that IC sensor systems powered by on-chip coils manufactured in this process technology, requiring a 1 V supply voltage and measuring $2 \times 2\text{mm}^2$ would not benefit of decreasing the power budget below 100 µW. Simulations show that such a power budget can be achieved at a transmitter power, P_{S}, of 25 dBm. If the discrepancy between simulated and measured results is accounted for, P_{S} amounts to 37 dBm or 5.0 W, which is a reasonable value for a PCB coil. These values are calculated for a power transfer efficiency of −43 dB.

We argue that a power budget of 100 µW is reasonable for our application; a temperature monitoring system for power semiconductor modules. As an example, using the temperature sensor presented in [19]—which consumes 14 µW at its highest operating temperature—would leave 86 µW for other on-chip systems such as rectifier, analogue-to-digital converter (ADC) and load modulator.

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