

Load-Dependent Power Transfer Efficiency for On-Chip Coils

Joakim Nilsson · Johan Borg · Jonny Johansson

the date of receipt and acceptance should be inserted later

Abstract This paper presents a theory for the power transfer efficiency of printed circuit board coils to integrated circuit coils, with focus on load-dependence for low-power single-chip systems. The theory is verified with electromagnetic simulations modelled on a 350 nm CMOS process which in turn are verified by measurements on manufactured integrated circuits. The power transfer efficiency is evaluated by on-chip rectification of a 151 MHz signal transmitted by a spiral coil on a printed circuit board at 10 mm of separation to an on-chip coil. Such an approach avoids the influence of off-chip parasitic elements such as bond wires, which would reduce the accuracy of the evaluation.

It is found that there is a lower limit for the load below which reducing the power consumption of on-chip circuits yield no increase in voltage generated at the load. For the examined process technology, this limit appears to lie around 56 k Ω . The paper is focused on the analysis and verification of the theory behind this limit.

Joakim Nilsson
Luleå University of Technology
Department of Computer Science, Electrical and Space Engineering
Luleå, Sweden
E-mail: joanil@ltu.se

Johan Borg
Imperial College
Department of Physics
London, United Kingdom
E-mail: j.borg@imperial.ac.uk

Jonny Johansson
Luleå University of Technology
Department of Computer Science, Electrical and Space Engineering
Luleå, Sweden
E-mail: jonny.johansson@ltu.se

We relate the results presented in this work to the application of wireless single-chip temperature monitoring of power semiconductors and conclude that such a system would be compatible with this limit.

Keywords condition monitoring · low power · near-field · on-chip coil · power semiconductor · wireless power transfer

1 Introduction

On-chip coils for wireless power transmission can be used to enable battery-free operation for integrated circuit systems such as implantable chips in humans [1–4] as well as for galvanically isolated, direct-contact temperature sensors for condition monitoring of power semiconductors [5, 6]. For integrated circuits powered by on-chip coils, it is important to achieve a sufficiently high power transfer efficiency (PTE), so that on-chip sensors' power requirements can be met without an excessive amount of power being consumed at the transmitter. However, the small dimensions of an on-chip coil limit its ability to draw energy from a magnetic field generated by a transmitter coil. Another limiting factor for the PTE is the typically low Q factors for such coils, resulting in a large amount of resistive losses occurring in the coils. For example, Zargham and Gulak [1], Feng *et al* [2], and Khalifa *et al* [3] demonstrate on-chip coils with Q factors of 11.05 at 101 MHz, 10.5 at 450.3 MHz, and 10.8 at 2.0 GHz, respectively. This is in contrast to printed circuit board (PCB) coils for which it has been demonstrated that their Q factors can exceed 100—or even 400 if advanced PCB substrates are employed [7].

One additional challenge is the load requirements and the limitations imposed by the associated on-chip

matching network. Because integrated circuit (IC) inductors with large inductance are difficult to manufacture with high Q factors, the matching network typically consists only of capacitors. Therefore any inductive part required by a matching network has to come from the on-chip receiver (Rx) coil. Because large load resistances require large inductors in order to be matched to the coil impedance, attempting to reduce the power consumption by reducing the load becomes ineffective beyond a certain point.

In this paper, we analyse the power transfer efficiency of systems powering on-chip coils with emphasis on the implications light loads (large load resistances) have on coil design. Focus is put on the implications for the power requirements of the transmitter. We evaluate the PTE by providing simulations for coil designs optimised for different loads and frequencies. In order to verify the simulation model, results of measurements are presented from an IC with an on-chip coil operating at 151 MHz, complete with a simple single-transistor half-wave rectifier. The on-chip rectification approach enables accurate measurements to be made at the Rx side because off-chip parasitic elements such as bond wires, probes and breakout tracks—which can be very significant at the frequency in question—are made irrelevant because off-chip currents are direct current (DC).

We assess the usefulness of the results presented in this work by relating them to the application of using wireless single-chip sensors to monitor the temperature of power semiconductors in a power semiconductor module, originally proposed in [5]. A schematic view of the proposed monitoring system is shown in Fig. 1. Single-chip temperature sensors with on-chip coils are glued in direct contact with the power semiconductors to provide accurate temperature measurements in order to predict emerging faults. The sensors are powered by and communicate with printed spiral coils (PSCs) located on a PCB on top of the power semiconductor module. The wireless interface provides galvanic isolation between IC sensors and a system controller located on the PCB outside the module housing. Monitoring of temperature can be used to predict solder fatigue [8], bond wire lift-off [9] or be a part in predicting emerging semiconductor faults [10, 11]. According to a 2007 study, these faults account for 34% of total failures in power electronic equipment [12].

The paper is organised as follows. In Section 2, we present an overview of how the power transfer efficiency is evaluated, including the measurement set-up and the placement of the different coils. In Section 3, we detail the circuits used to model the coils and derive a theoretical limit for when the required transmitter power does not decrease even if the power consumption at the load

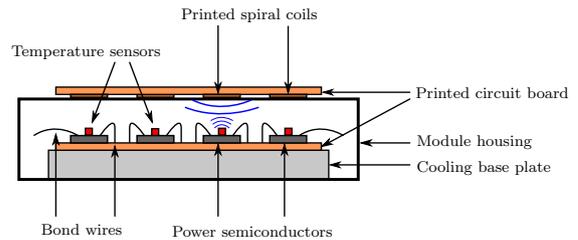


Fig. 1 Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by printed spiral coils mounted on top of the module.

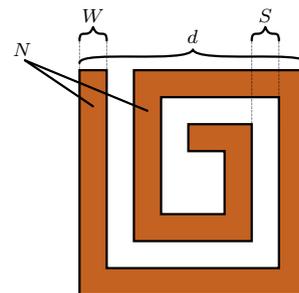


Fig. 2 Schematic diagram of a printed spiral coil. Shown are the geometry parameters, tracewidth, W ; trace separation, S ; outer diameter, d ; and number of turns, N used to describe its geometry.

is reduced. Section 4 presents simulations of optimised coil geometries supporting the theory. These simulations are verified by measurements on manufactured devices and the results of the measurements are presented in Section 5. Conclusions are presented in Section 6.

2 System Overview

In this section, we describe the measurement set-up used to evaluate the power transfer efficiency between two coupled coils: a transmitter (Tx) spiral coil printed on a PCB and an Rx spiral coil printed on an IC chip utilising a 350 nm complementary metal-oxide semiconductor (CMOS) process. The measurements are used to verify the simulation model presented in Section 4. Both Tx and Rx coils are PSCs characterised by outer dimension, d_X ; trace width, W_X ; trace separation, S_X ; and number of turns, N_X . Here, X denotes either the receiver coil, Rx, or the transmitter coil, Tx. These parameters are illustrated in the schematic diagram of Fig. 2. The power transfer efficiency is evaluated at a coil separation of $D = 10$ mm, which is a reasonable distance both for biomedically implanted chips [1] and for sensor chips for condition monitoring of power semiconductors [6].

An overview of the measurement set-up is shown in Fig. 3. The excitation signal is generated using a Prāna

APT32MT225 Power Amplifier driven by a sinusoid which is generated by an Agilent E8267D Signal Generator. The power signal is attenuated by 6 dB by a power attenuator and the attenuated signal is fed to a Mini-Circuits ZFBDC20-62HP-S+ directional coupler from which -20 dB is coupled to and measured by an Anritsu ML2437A power meter. The output of the coupler is fed to a PCB with the Tx coil. Any reflected power from the PCB is fed back to the directional coupler from which -20 dB is coupled to another ML2437A power meter. Using the two power measurements, the power, P_S , delivered to the PCB can be calculated.

An inductive link is formed by the two coils, and a fraction of the signal power fed to the Tx coil is coupled to the Rx coil. In the following, this system is described in more detail:

2.1 Transmitter Printed Circuit Board

On the Tx side, a PSC is printed on a PCB with a discrete LC matching network to enable sufficient power to be delivered to the Tx coil at the operating frequency. The matching network consists of a series variable capacitor and a shunt inductor. Because of the low equivalent series resistance (ESR) of the transmitting coil, losses in the matching components may be significant.

2.2 Receiver Chip

On the Rx side, a PSC is printed on a 2×2 mm² IC chip using the two top metal layers. Because large on-chip inductors require large area and typically exhibit low Q factors, the matching network consists of a single on-chip shunt capacitor, which forms a resonant circuit with the Rx inductor.

The integrated circuit includes a single-transistor half-wave rectifier, the purpose of which is to increase the accuracy of the measurements by rectifying on-chip and thus making the system less sensitive to parasitic effects. Such effects include magnetic coupling from the Tx coil to bond wires and PCB tracks as well as parasitic capacitance between such elements and within coaxial cable connectors. The simplicity of a single-transistor rectifier enables accurate estimation of its power consumption. It is thus possible to separate the power consumed in the rectifier from the power, P_L , consumed in the load, obtaining estimations of both.

Excluding the IC coil which runs along the chip's perimeter, the rectifier consumes 54 nm² of silicon area. The total area consumed by the coil amounts to 346 nm²

2.3 Inductive Link and Rectification

A circuit diagram of the two coupled Tx and Rx coils is shown in Fig. 4 complete with matching networks, rectifier and load. An inductive link is formed between the Tx coil, L_{Tx} , and the Rx coil, L_{Rx} , coupled by the mutual inductance, M . $L_{m,Tx}$ and $C_{m,Tx}$ constitute the matching network on the Tx side while the single shunt capacitor, $C_{m,Rx}$, constitutes the matching network on the Rx side. The metal-oxide semiconductor field effect transistor (MOSFET), M_D , is configured as a PMOS diode which rectifies the voltage induced in L_{Rx} . The rectified energy is used to drive a load resistor, R_L , external to the chip. Energy not consumed in the load is stored in the energy-storage capacitor, C_E , and used to drive the load when M_D is reverse-biased. Also shown is the equivalent resistance, R'_L , due to the average loading of coil with matching network, which is the sum of R_L and the average equivalent resistance of the rectifier. The DC value of the load voltage, V_L , is buffered by an Analog Devices ADA4505 operational amplifier in voltage follower configuration and then sampled by an Agilent MSOX2024A oscilloscope. With the sampled voltage, the power, P_L , consumed at the load can be estimated.

3 Coil Modelling and Design

In this section we describe the electromagnetic situation for the monitoring system shown in Fig. 1. A theory is presented demonstrating the effect that the loading of the on-chip coil has on transmitter power consumption. We argue that decreasing the load (that is increasing the load resistance) beyond a certain point has a negative impact on the power transfer efficiency which precisely cancels out the positive effect of a lower current consumption at the load. The result is that, beyond this point, the transmitter power required in order to realise a constant voltage at the load does not decrease even if the load is reduced.

In Section 4, we present simulation results to support the theory. These results are obtained from an optimisation algorithm that uses an electromagnetic simulator that generates optimised coil-designs for varying loads and frequencies.

3.1 On-Chip Coil Circuit Model

The on-chip coil is modelled as in Fig. 5. Here, $\mathbf{V}_{emf}(j\omega)$ is the electromotive force (emf) voltage phasor induced in the Rx coil from the magnetic field generated by the Tx coil. L_{Rx} is the coil inductance and R_{Rx} is the

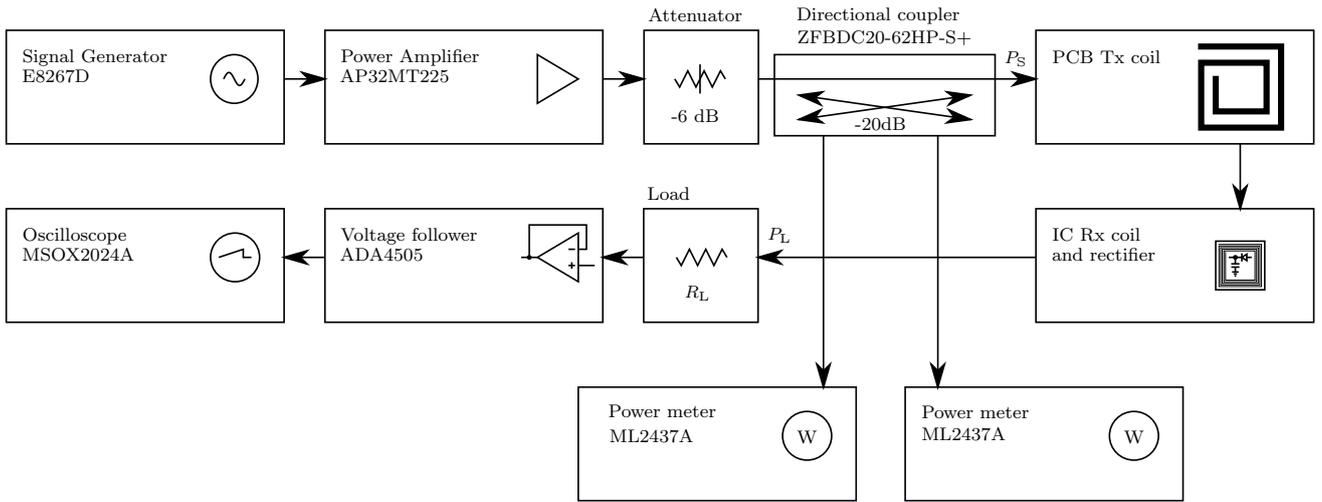


Fig. 3 Overview of the measurement set-up used to verify the electromagnetic model used for simulations. A sinusoidal E8267D signal generator drives a APT32MT225 power amplifier. The signal is then attenuated by 6 dB and the attenuated signal is fed to a ZFBDC20-62HP-S+ directional coupler from which -20 dB is coupled to and measured by an ML2437A power meter. The output of the coupler is fed to the PCB Tx coil and any reflected signal is fed back to the directional coupler and -20 dB of the reflected signal is measured by another ML2437A power meter. Power is transferred inductively from the PCB Tx coil to the IC Rx coil where the signal is rectified and fed to a load. The voltage at the load is buffered by an ADA4505 operational amplifier in voltage follower configuration and then sampled by an MSOX2024A oscilloscope.

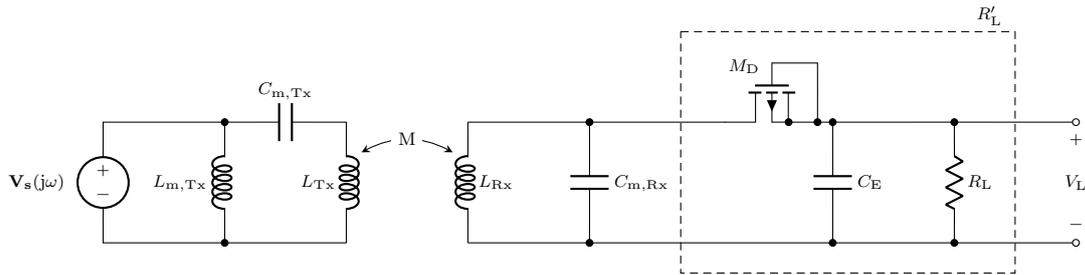


Fig. 4 Schematic diagram of a PCB coil inductively coupled to a IC coil with on-chip single-transistor rectifier. The schematic also includes matching components and load resistance.

ESR of the coil due to the combined effects of non-zero resistance of the metal constituting the coil and due to resistive losses in the silicon substrate due to induced substrate current (and current induced in a substrate shield). C_{sub} and R_{sub} represent equivalent capacitance and resistance due to capacitive coupling to the ground-connected conductive substrate while C_{turn} represents the equivalent capacitance between turns. This is a simplified model whose purpose is to yield design insight of how the coil geometry affects the properties of the final coil.

The dependencies of the Rx model parameters, V_{emf} , R_{Rx} , L_{Rx} , R_{sub} , C_{sub} and C_{turn} on the Rx geometry parameters, W_{Rx} , S_{Rx} and N_{Rx} are summarised in Table 1. Here, V_{emf} is the amplitude of the emf voltage phasor, $\mathbf{V}_{\text{emf}}(j\omega)$.

For thin, long conductors, the inductance increases with the logarithm of W_{Rx} [13], while the ESR decreases

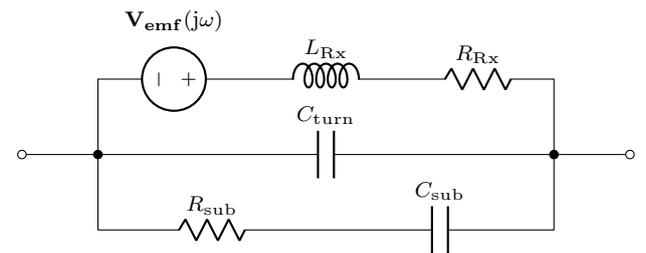


Fig. 5 Circuit used to model an on-chip coil.

inversely proportionally to W_{Rx} . The skin effect is assumed negligible because of the small thickness of the IC metal layers. Because of the increase in total surface-area consumed by the coil, increasing W_{Rx} results in that the coil will be capacitively coupled to a larger fraction of the substrate, decreasing R_{sub} and increasing C_{sub} . S_{Rx} has a similar effect on R_{sub} and C_{sub} due to increasing coil area, while also decreasing the inter-

Table 1 Model parameter dependencies on geometry parameters. Here, “-” denotes no or insignificant dependence, \nearrow denotes a function that increases with the geometry parameter, while \searrow denotes a decreasing relation.

Model param.	Dependency on geom. param.		
	W_{Rx}	S_{Rx}	N_{Rx}
V_{emf}	\searrow	\searrow	$\nearrow (N_{\text{Rx}})$
L_{Rx}	$\nearrow (\log W_{\text{Rx}})$	-	$\nearrow (N_{\text{Rx}}^2)$
R_{Rx}	$\searrow (W_{\text{Rx}}^{-1})$	-	$\nearrow (N_{\text{Rx}}, N_{\text{Rx}}^2)$
R_{sub}	\searrow	\searrow	\searrow
C_{sub}	\nearrow	\nearrow	\nearrow
C_{turn}	-	$\searrow (S_{\text{Rx}}^{-1})$	\nearrow

turn capacitance roughly inversely proportionally to S_{Rx} . N_{Rx} increases the induced emf voltage in the coil roughly linearly [14], while the coil inductance increases roughly proportionally to the square of N_{Rx} [15]. We say roughly because the diameter of each turn is not uniform for a printed spiral coil, nor is the coil circular and hence the assumption of an ideal coil is an approximation. Because the inner turns will attain smaller diameters if either W_{Rx} or S_{Rx} is increased, V_{emf} will decrease slightly for such a case. Additionally, increasing N_{Rx} adds a roughly linear term to the ESR because the coil gets longer roughly proportionally to the number of turns. Furthermore, because the inductive coupling to substrate or substrate shield increases with the square of the number of turns [16], another term, N_{Rx}^2 , is added to R_{Rx} .

It is assumed that the optimised coil geometries will have values for the turn separation of the Rx coil, S_{Rx} , that makes the effect of the inter-turn capacitance on the power delivered to the load small and thus, this effect is ignored henceforth. Furthermore, we do not attempt to estimate values for C_{sub} and R_{sub} due to the complexity of such a task, but merely discuss the limitations the effect as a whole imposes on the coil design. Thus, for calculations, we assume that the effects of C_{sub} and R_{sub} are represented in $\mathbf{V}_{\text{emf}}(j\omega)$, L_{Rx} and R_{Rx} .

3.2 Maximum Load Resistance

As explained in Section 2.2, the on-chip matching network consists of a single shunt capacitor. A series capacitor would cancel out the reactance of the coil, while a shunt capacitor would cancel the coil reactance, but also transform the load resistance into a smaller one. For low-power operation, the load resistance is assumed to be larger than the magnitude of the source impedance given by the ESR of the Rx coil in series with the coil reactance. Thus, in order to bring the load resistance as close as possible to the magnitude of the source impedance—in an effort to maximise the power deliv-

ered to the load—the matching network consist of a shunt capacitor, as illustrated in Fig. 4.

To simplify the analysis and without loss of generality, the average equivalent load resistance, R'_L , is used for calculations.

The power, P_L , delivered to the average equivalent load, R'_L is given by

$$P_L = \left| \mathbf{V}_{\text{emf}}(j\omega) \frac{Z_{\text{eq}}}{Z_{\text{eq}} + R_{\text{Rx}} + j\omega L_{\text{Rx}}} \right|^2 / R'_L, \quad (1)$$

where $\mathbf{V}_{\text{emf}}(j\omega)$ is the input voltage phasor generated in the Rx coil by the signal transmitted from the Tx coil, ω is the angular operating frequency and Z_{eq} is the equivalent impedance from the parallel connection formed by $C_{\text{m,Rx}}$ and R'_L , given by

$$Z_{\text{eq}} = \frac{R'_L / j\omega C_{\text{m,Rx}}}{R'_L + 1/j\omega C_{\text{m,Rx}}} = \frac{R'_L - j\omega C_{\text{m,Rx}} R'^2_L}{\omega^2 C^2_{\text{m,Rx}} R'^2_L + 1}. \quad (2)$$

By substituting Eq. (2) into Eq. (1), it can be shown that P_L can be expressed as

$$P_L = V_{\text{emf}}^2 \frac{R'_L}{R'^2_L [1 + \omega^2 C^2_{\text{m,Rx}} (R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}) - 2\omega L_{\text{Rx}} \omega C_{\text{m,Rx}}] + R^2_{\text{Rx}} + 2R'_L R_{\text{Rx}} + \omega^2 L^2}, \quad (3)$$

where V_{emf} is the amplitude of the input voltage phasor, $\mathbf{V}_{\text{emf}}(j\omega)$.

It can be seen from Eq. (3) that for a fixed on-chip coil design (fixed values for V_{emf} , R'_L , R_{Rx} , L_{Rx} and ω), in order to maximise P_L , the expression

$$f(\omega C_{\text{m,Rx}}) = \omega^2 C^2_{\text{m,Rx}} (R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}) - 2\omega L_{\text{Rx}} \omega C_{\text{m,Rx}} \quad (4)$$

should be minimised. Because

$$\frac{d^2 f(\omega C_{\text{m,Rx}})}{d(\omega C_{\text{m,Rx}})^2} = 2 (R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}) \quad (5)$$

is positive,

$$\frac{df(\omega C_{\text{m,Rx}})}{d(\omega C_{\text{m,Rx}})} = 2\omega C_{\text{m,Rx}} (R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}) - 2\omega L_{\text{Rx}} = 0 \quad (6)$$

yields a local minimum point for $\omega C_{\text{m,Rx}}$; namely

$$\omega C_{\text{m,Rx}} = \frac{\omega L_{\text{Rx}}}{R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}}. \quad (7)$$

Inserting Eq. (7) into Eq. (3) yields

$$P_{L,\text{max}} = V_{\text{emf}}^2 \frac{R'_L}{\gamma R'^2_L + 2R'_L R_{\text{Rx}} + R^2_{\text{Rx}} + \omega^2 L^2_{\text{Rx}}}, \quad (8)$$

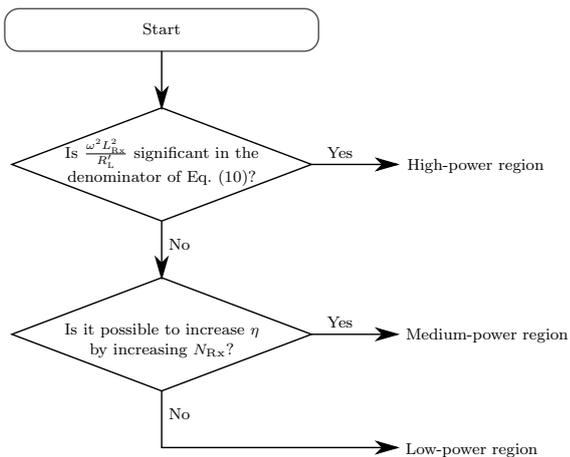


Fig. 6 Flowchart illustrating the conditions for the different regions of operation regarding power for a coupled PCB-IC coil system with a single on-chip shunt capacitor as matching network at the IC side.

where

$$\gamma = 1 - \frac{\omega^2 L_{Rx}^2}{R_{Rx}^2 + \omega^2 L_{Rx}^2} = \frac{1}{Q_{Rx}^2 + 1}, \quad (9)$$

where $Q_{Rx} = \omega L_{Rx}/R_{Rx}$ is the Q factor of the Rx coil. Assuming a reasonably high Q_{Rx} , $\omega^2 L_{Rx}^2 \gg R_{Rx}^2$, Eq. (8) reduces to

$$P_{L,max} \approx \frac{V_{emf}^2}{\gamma R_L' + 2R_{Rx} + \omega^2 L_{Rx}^2/R_L'}. \quad (10)$$

$P_{L,max}$ in Eqs. (8) and (10) represent the maximum obtainable power for a fixed on-chip coil design assuming an ideal matching capacitor, $C_{m,Rx}$. A method for manufacturing trimmable, high Q factor IC capacitors which can be utilised in order to approximate such a capacitor has been proposed in [17]. As can be seen from Eq. (9), γ will decrease with increasing Q factor. Thus for high Q factors, R_L' will be less significant for $P_{L,max}$ and in turn for the power transfer efficiency, $\eta = P_{L,max}/P_S$. Based on observed IC coil Q factors from this and previous works [1, 2], for optimised coils, γ typically attains values of around 0.6-10 %.

In the following, we will show that the coupled PCB-IC coil system of this paper operates in three different regions of operation characterised by the power consumption at the load. We denote these regions the *high-power*, *medium-power* and *low-power* regions of operation. The conditions for these regions are illustrated in the form of a flowchart in Fig. 6, and the remainder of this section is devoted to analysing their characteristics and conditions.

As noted in Table 1, the induced voltage amplitude, V_{emf} , is roughly proportional to the number of turns in the receiver coil, N_{Rx} , while the inductance, L_{Rx} ,

is roughly proportional to N_{Rx}^2 . Thus, Eq. (10) shows that increasing N_{Rx} beyond the point where $\omega^2 L^2/R_L'$ starts to become dominant will reduce the maximum power delivered to the load, $P_{L,max}$. We say that the system transitions from operating in the high-power region to the medium-power region at this point. Due to the previous reasoning, it can thus be assumed that for an optimal coil design, $\omega^2 L_{Rx}^2/R_L' \ll \gamma R_L' + 2R_L'$ and Eq. (10) reduces to

$$P_{L,max} \approx \frac{V_{emf}^2}{\gamma R_L' + 2R_{Rx}}. \quad (11)$$

However, it should be noted that this assumption ignores the fact that the number of turns must be a non-zero integer. The assumption may thus be false for designs with few turns for which the impedance, $\omega^2 L_{Rx}^2/R_L'$, (the values of which are quantised for a constant R_L' due to the quantised nature of N_{Rx}) may be excessively small compared to $2R_{Rx}$. Thus for some designs, a unit increment in N_{Rx} would result in an increase in $P_{L,max}$ because, for some cases, the benefit of a higher V_{emf} would actually be bigger than the drawback of a higher $\omega^2 L_{Rx}^2$. Thus for medium-power operation, the approximation given in Eq. (11) is valid, but for high-power operation, it may be invalid and we should resort to using Eq. (10).

Because $\omega^2 L_{Rx}^2/R_L'$ will dominate the denominator of Eq. (10) only for small values of R_L' , it is only relevant for high-power operation, which is not the focus of this work. However, it should nonetheless be noted that because $\omega^2 L_{Rx}^2/R_L'$ is significantly more detrimental for $P_{L,max}$ than is $\gamma R_L'$ in this region of operation, it would be more beneficial to employ a series capacitor matching network which would fully cancel the coil reactance. The maximum power consumption for series matching network would then be given by Eq. (8), but with $\gamma = 1$ and $\omega L_{Rx} = 0$, that is

$$P_{L,max,series} = V_{emf}^2 \frac{R_L'}{R_L'^2 + 2R_L' R_{Rx} + R_{Rx}^2}. \quad (12)$$

The drawback here is that the $R_L'^2$ term in the denominator of Eq. (8) is no longer reduced by a factor γ and thus, if $R_L'^2$ is dominant, the power delivered to the load will be reduced, again illustrating that a series-capacitor topology is sub-optimal for medium- and low-power operation.

For medium-power operation, $\omega^2 L_{Rx}^2/R_L'$ will no longer be dominant in the denominator of Eq. (11). Thus, in this region, the more R_L' is increased, the more N_{Rx} can grow without being detrimental for $P_{L,max}$. From Eq. (11) and Table 1, it can be seen that a linear increase in N_{Rx} yields a roughly quadratic increase in $P_{L,max}$ due to the resulting increase in V_{emf} . However,

R_{Rx} will increase roughly linearly, which is detrimental for $P_{\text{L,max}}$, but is detrimental to a smaller extent than the increase in V_{emf} is beneficial for $P_{\text{L,max}}$. A linear increase in R_{Rx} will also result in a roughly quadratic increase in γ due to the Q_{Rx}^2 term in the denominator of Eq. (9). Nevertheless, because of the typically low Q factors of on-chip coils, the unity term in the denominator of Eq. (9) may be significant, resulting in an overall reduction in γ that is less than quadratic and which can thus be less detrimental for P_{L} than the quadratic increase in V_{emf} . Therefore, W_{Rx} can decrease slightly, in turn increasing V_{emf} slightly because of the increased radii of the inner turns, without the resulting increase in R_{Rx} consequentially resulting in that $2R_{\text{Rx}}$ becomes the dominant term in the denominator of Eq. (11) and without scaling up γ by more than by how much V_{emf}^2 was scaled. A consequence of this behaviour is that, when the power transfer efficiency, $\eta = P_{\text{L,max}}/P_{\text{S}}$, decreases due to increasing R'_{L} , the power delivered to the load, $P_{\text{L,max}}$, can still increase (for the same transmitted power, P_{S}) due to the boosts in V_{emf} resulting from an increased number of turns and increasing diameters of the inner turns due to a smaller trace width.

However, there is a limit for the load resistance for when increasing the number of turns, N_{Rx} , will stop being beneficial for $P_{\text{L,max}}$. Because of the diminishing returns in the increase in V_{emf} due to the increasingly smaller radii of the inner turns when an additional turn is employed, and the increasingly limiting effects of the substrate when the fill factor of the coil is increased, beyond this limit, which we denote $R_{\text{L,cutoff}}$, an increase in N_{Rx} will instead be detrimental for $P_{\text{L,max}}$. For values for $R'_{\text{L}} > R_{\text{L,cutoff}}$, the strategy of increasing R'_{L} in an attempt to move towards lower power operation becomes ineffective because $P_{\text{L,max}}$, and in turn η , are reduced with the same factor as the load current (which is given by $V_{\text{L}}/R'_{\text{L}}$). The implication is that, beyond this point, reducing the load current does not significantly increase the available supply voltage, V_{L} , for a given V_{emf} .

When N_{Rx} no longer can be increased, the benefits by a decrease in W_{Rx} seen for medium-power operation will no longer apply and the coil geometry will thus not vary much in the region of low-power operation. Consequentially, in the low-power region, $2R_{\text{Rx}}$ will no longer increase and $\gamma R'_{\text{L}}$ will be dominant in the denominator of Eq. (11). Therefore, $\gamma R_{\text{L}} \gg 2R_{\text{Rx}}$ and Eq. (11) can be approximated by

$$P_{\text{L,max}} \approx \frac{V_{\text{emf}}^2}{\gamma R'_{\text{L}}}. \quad (13)$$

Because of the coil geometry invariance in the low-power region of operation, a viable strategy for finding $R_{\text{L,cutoff}}$ may be to determine the impedance of an

optimised coil geometry for a high R'_{L} (well into the low-power region), and use the result to calculate values for the impedances $\gamma R'_{\text{L}}$ and $2R_{\text{Rx}}$. At the transition from medium-power to low-power operation, $2R_{\text{Rx}}$ will stop being significant, and thus at this point, it can be assumed that $2R_{\text{Rx}}$ will be only slightly smaller than $\gamma R'_{\text{L}}$. We denote the fraction that relates $\gamma R'_{\text{L}}$ to $2R_{\text{Rx}}$ as β . Thus, for low power operation:

$$2R_{\text{Rx}} = \beta \gamma R'_{\text{L}}. \quad (14)$$

The cut-off point, $R_{\text{L,cutoff}}$ can then be found by substituting $R'_{\text{L}} = R_{\text{L,cutoff}}$ into Eq. (14) and solving for $R_{\text{L,cutoff}}$. $R_{\text{L,cutoff}}$ is then given by

$$R_{\text{L,cutoff}} = \frac{2R_{\text{Rx}}}{\beta \gamma} = \frac{2R_{\text{Rx}}}{\beta} (Q_{\text{Rx}}^2 + 1). \quad (15)$$

Towards the end of Section 4, we will empirically determine a suitable value for β .

4 Coil Geometry Optimisation for Varying Load

A gradient ascent algorithm was used in conjunction with the electromagnetic simulator FEKO [18] in order to optimise the coil geometries for high power transfer efficiency. The algorithm is the same as from our earlier work [6], based on an algorithm originally presented by Zargham and Gulak [1]. Pseudo-code for the algorithm is repeated for reference in this work in Algorithm 1.

For the electromagnetic simulations, an IC chip was modelled in direct contact with a power semiconductor inside a module as shown in Fig. 1. An extended version of the schematic including material information is shown in Fig. 7, while permittivities and conductivities for the materials are listed in Table 2. In order to shorten simulation times, the model was simulated in 2.5-dimensional (2.5D) mode, where the layers of the different materials are modelled as infinite slabs in the horizontal direction. A 350 nm, 3.3 V process (C3B4C3 from ams AG) with 4 metal (copper) layers was used. Out of these layers, the top 2 layers, metal 3 and metal 4 were used for the coil, stitched together with vias at the corners, realising a parallel connection. The bottom metal layer, metal 1, was used to shield the on-chip coil from the conductive substrate [1]. The shield consist of a chopped-up coil laid out directly underneath the Rx coil.

The coil geometries were optimised in order to maximise the power transfer efficiency, η , for different average equivalent load resistances, R'_{L} , a coil separation of $D = 10$ mm and an outer diameter for the Rx coil of $d_{\text{Rx}} = 2$ mm. In order to assess which is the most favourable frequency, simulations were first run in order

Algorithm 1 Power transfer efficiency optimisation algorithm for coil geometries. Originally published in [6] and based on [1].

Step 1: Initialisation
$N_{Tx} := 1$
$W_{Tx} :=$ minimum allowed PCB trace width
$S_{Tx} :=$ minimum allowed PCB trace separation
$d_{Tx} := D \cdot \sqrt{2(1 + \sqrt{5})}$
$N_{Rx} := 1$
$W_{Rx} :=$ minimum allowed chip trace width
$S_{Rx} :=$ minimum allowed chip trace separation
$d_{Rx} :=$ chip die size
Step 2: Tx coil quality factor optimisation
for $1 \leq N_{Tx} \leq 15$:
gradient ascent algorithm:
search: N_{Tx}, W_{Tx}, S_{Tx}
maximise: Q_{Tx}
update: N_{Tx}, W_{Tx}, S_{Tx} for maximum Q_{Tx}
Step 3: Rx coil quality factor optimisation
for $1 \leq N_{Rx} \leq 15$:
gradient ascent algorithm:
search: N_{Rx}, W_{Rx}, S_{Rx}
maximise: Q_{Rx}
update: N_{Rx}, W_{Rx}, S_{Rx} for maximum Q_{Rx}
Step 4: Tx coil power transfer efficiency optimisation
for $1 \leq N_{Tx} \leq 15$:
gradient ascent algorithm:
search: $N_{Tx}, W_{Tx}, S_{Tx}, d_{Tx}$
maximise: η
update: $N_{Tx}, W_{Tx}, S_{Tx}, d_{Tx}$ for maximum η
Step 5: Rx coil power transfer efficiency optimisation
for $1 \leq N_{Rx} \leq 15$:
gradient ascent algorithm:
search: N_{Rx}, W_{Rx}, S_{Rx}
maximise: η
update: N_{Rx}, W_{Rx}, S_{Rx} for maximum η
Step 6: Stop condition
if η improved since step 4:
go to Step 4
else:
stop

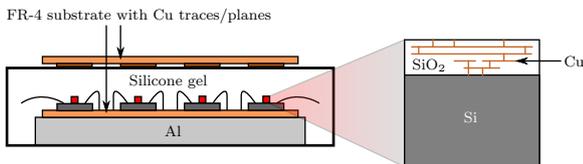


Fig. 7 Material information for the monitoring system shown in Fig. 1.

Table 2 Material properties for the materials used in this work.

Material	Relative permittivity	Conductivity [MS/m]
Silicon substrate	11.7	not available*
Silicon dioxide	3.9	~ 0
Silicone gel	2.1	~ 0
FR-4	4.4	~ 0
Copper	1	59.6

*Value known and used for simulations, but can not be published due to non-disclosure agreement.

to optimise η for $R'_L = 100 \text{ k}\Omega$. The frequency bands 44.66, 169.4, 433.0 and 868.0 MHz were examined. These are industrial, scientific and medical (ISM) bands or other frequency bands recommended by the Swedish post and telecommunications authority [19]. Out of these, 169.4 MHz yielded the highest power transfer efficiency at $\eta = -45.5 \text{ dB}$, and so, the remainder of the simulations presented in this section were carried out at this frequency¹.

To visualise the characteristics of the best values of power transfer efficiency, the coil geometries were optimised to maximise η for various values of R'_L . The best values found by the optimiser are shown in Figs. 8 and 9, where the power transfer efficiency and its corresponding Rx coil geometry, respectively, are plotted against R'_L . Also shown are the high-power, medium-power and low-power regions of operation as described in Section 3.2. From Fig. 8 it can be seen that the maximum power transfer efficiency occurs in the high-power region, around $R'_L = 180 \Omega$. We comment on the Rx coil dimensions in relation to power transfer efficiency later in this section. The optimisation algorithm yielded roughly the same geometry for the Tx coil for all the examined average equivalent load resistances and thus we present its geometry and Q factor for the arbitrarily chosen value of $R'_L = 10 \text{ k}\Omega$ in table form in Table 3. The lack of variation is expected due of the weak coupling between the coils which results in that the effect of the loading of the Rx side is not very significant for the Tx coil.

In the following paragraphs, we assume that the optimiser has found near-optimal coil geometries. Fig. 10 shows plots of the impedances of the terms in the de-

¹ We should note that this frequency differs from the one obtained in our earlier work; 433 MHz [6]. The reason for this is a previous error in the model which placed the substrate farther apart from the copper traces than it should have been, resulting in underestimated substrate effects. This error has since been corrected and the corrected version is used for the simulations in this work. As a result of the error, the results obtained in our previous work also overestimates the power transfer efficiency. The power transfer efficiencies shown in this work are verified against measurements and are thus believed to be accurate.

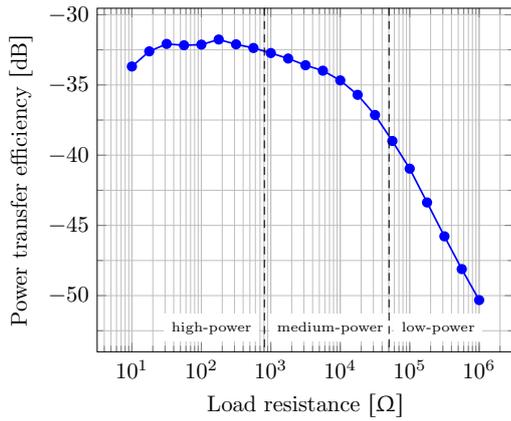


Fig. 8 Power transfer efficiency of coils optimised for different average equivalent load resistances.

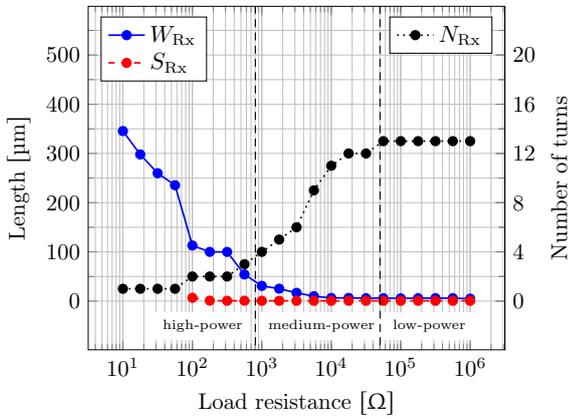


Fig. 9 Optimised geometry of the Rx coil plotted as a function of average equivalent load resistance. The trace separation is undefined for coil geometries with only a single turn, which is why values are missing for S_{Rx} for load resistances smaller than 100 Ω .

Table 3 Optimised coil geometry and Q factor for the Tx coil at a load resistance of 10 k Ω .

Parameter		Value
Trace width,	W_{Tx}	3.0 mm
Trace separation,	S_{Tx}	1.5 mm
Outer dimension,	d_{Tx}	25.4 mm
No. of turns,	N_{Tx}	2
Q factor @ 169.4 MHz (simulated)	Q_{Tx}	139.4

nominator of Eq. (10) as a function of load resistance. Looking at both the figure and the equation, it can be seen that $\omega^2 L_{Rx}^2 / R'_L$ stops being significant for $P_{L,max}$ at around $R'_L = 320 \Omega$. Looking back at Fig. 8 it can be seen that it is around this point that η starts to fall off, and at around $R'_L = 56 \text{ k}\Omega$, the maximum decline of 10 dB per decade increase in R'_L is reached. As argued in Section 3.2, it is beyond this point that, for a constant load voltage, there is no reduction in the required transmitter power, P_S , even if an attempt to reduce it is made by increasing R'_L because the current

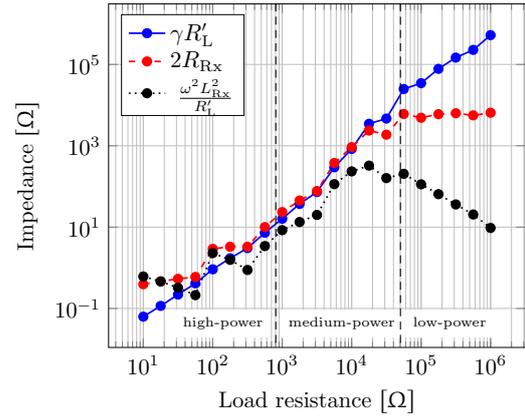


Fig. 10 Magnitude of the impedance terms in the denominator of Eq. (10) for the Rx coil optimised at different average equivalent load resistances.

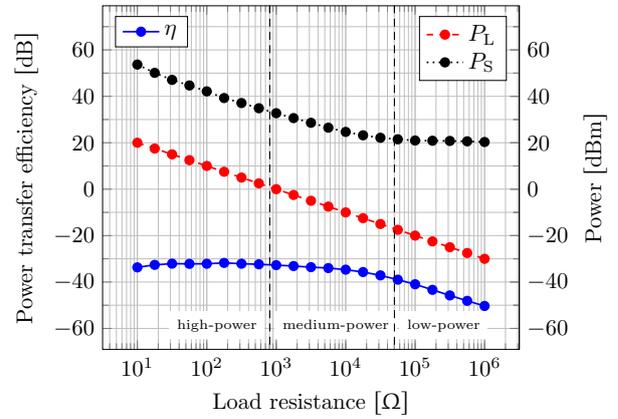


Fig. 11 Power transfer efficiency, η , transmitted power, P_S , and consumed power, P_L , for coils optimised for different equivalent average load resistances. P_S is the power delivered to the transmitting coil required in order to maintain an rms voltage of 1 V over the load, while P_L is the power consumed at the load.

consumption—and hence the power delivered to the load, P_L —decrease at the same rate as does the power transfer efficiency, η . This phenomenon can be seen in Fig. 11. Here, both P_L and η are plotted as functions of load resistance, and the figure also plots the power consumption of the transmitting coil, P_S , required in order to realise a root-mean-square (rms) load voltage, V_L , of 1 V. The purpose of presenting plots for constant V_L is to uncover the behaviour of P_L when the current consumption is solely dependent on load resistance. The figure shows that the required transmitting power decreases up to the point where the plotted slopes of P_L and η become equal, at which point P_S starts to level off, asymptotically reaching a constant value of around 20 dBm at around $R'_L = 56 \text{ k}\Omega$.

It is interesting to analyse Figs. 9, 10 and 11 further. It can be seen that in the region of high-power opera-

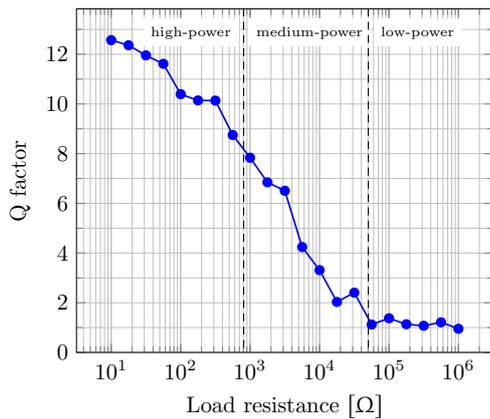


Fig. 12 Simulated Q factor of the Rx coil optimised for different load resistances.

tion, where $R'_L < 320 \Omega$, either $2R_{Rx}$ or $\omega^2 L_{Rx}^2 / R'_L$ is dominant and L_{Rx} must be kept low in order to not be detrimental for P_L . Because of the strong dependence of L_{Rx} on N_{Rx} , N_{Rx} will be kept low in this region as can be seen from Fig. 9. An exception is $R'_L = 100 \Omega$, where it turns out that increasing N_{Rx} by one turn was more beneficial for P_L due to the increase in V_{emf} than it was detrimental due to the increase in L_{Rx} . However, when $\omega^2 L_{Rx}^2 / R'_L$ is surpassed by both $\gamma R'_L$ and $2R_{Rx}$, L_{Rx} can grow without a reduction in P_L and the system transitions into the medium-power region of operation. A consequence is that N_{Rx} starts growing steadily at around $R'_L = 320 \Omega$ after which $\omega^2 L_{Rx}^2 / R'_L$ never again becomes dominant. N_{Rx} grows until it reaches a maximum of $N_{Rx} = 11$ where additional turns will be detrimental to P_L —due to the diminishing returns in inductance for additional turns and to stronger substrate effects—more than it will benefit P_L due to the increase in V_{emf} .

Fig. 12 shows the Q factors resulting from optimising the Rx coil for different average equivalent load resistances, R'_L . The figure shows that while the Q factor is relatively high for low R'_L , it rapidly drops off in the medium-power region of operation and eventually reaches a minimum of $Q_{Rx} \approx 1$ when the system reaches the low-power region. This behaviour is expected because the number of turns, N_{Rx} is fairly constant in the high- and low-power regions, while steadily increasing in the medium-power region. A high number of turns will decrease Q_{Rx} because the trace width, W_{Rx} , will decrease to accommodate the additional turns. On top of this, because the inner turns have smaller diameters compared to the outer one, the increase in inductance will diminish as N_{Rx} grows larger, further decreasing the Q factor.

Fig. 9 shows that S_{Rx} remains fairly constant throughout the entire load resistance range. An explanation for this could be that the value S_{Rx} attains simply makes

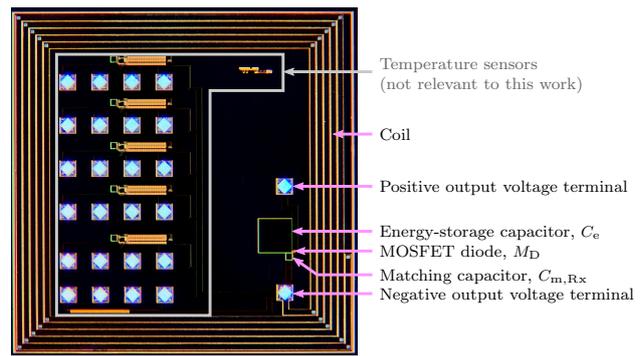


Fig. 13 Microphotograph of the IC used for the measurements presented in this work.

the inter-turn capacitance, C_{turn} , negligible for the frequency in question.

Furthermore, in order to estimate a suitable value for β in Eq. (15), Eq. (14) is solved for β and values for $\gamma R'_L$ and $2R_{Rx}$ are obtained from Fig. 10 at the observed transition to the low-power region, at $R'_L = 56 \text{ k}\Omega$. By this procedure, a value of $\beta = 0.24$ is obtained. Using this value for β , in order to test the validity of the theory on how to estimate $R_{L,cutoff}$, values for $\gamma R'_L$ and $2R_{Rx}$ are taken from Fig. 10 at $R'_L = 1 \text{ M}\Omega$ and inserted into Eq. (15). The result is $R_{L,cutoff} = 51 \text{ k}\Omega$ —reasonably close to the observed cut-off point at $R_{L,cutoff} = 56 \text{ k}\Omega$.

5 Measurements

In this section we present measurements used to confirm the validity of the simulations presented in the previous section.

5.1 MOSFET Diode Characterisation

In order to accurately estimate the power transfer efficiency, η , of the system described in Section 2, the MOSFET diode, M_D , was characterised. This was done by sweeping the DC current of a Keithley 2450 source meter while monitoring the resulting voltage. The result is presented in Fig. 14. The figure reveals a forward voltage, V_D , of between 500 and 750 mV for a forward current between 10 and 1000 μA .

5.2 Power Transfer Efficiency Characterisation for Varying Load Resistance

An experimental set-up was arranged according to Fig. 3 with a matched PCB coil driven by a power amplifier. An IC containing an on-chip coil, a shunt capacitor

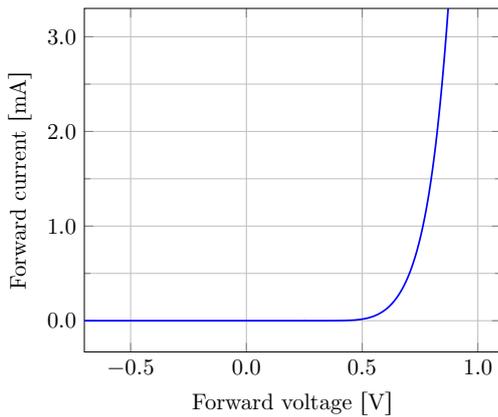


Fig. 14 Measured current–voltage characterisation of the MOSFET diode, M_D .

as matching network and a rectifier was manufactured in a 350 nm CMOS process and is modelled on the optimised design presented in our previous work, [6]. A microphotograph of the IC layout is presented in Fig. 13. This is a 5-turn coil with a trace width of $35\ \mu\text{m}$, a trace separation of $6.0\ \mu\text{m}$ and an outer diameter of 2.0 mm. Although that design turned out to be sub-optimal due to a previous error in the simulation model as detailed in Section 4, we use that design in this work in order to verify our now corrected simulation model. In addition to coil, matching network and rectifier, the IC also hosts temperature sensors which are not relevant to this work, but included to utilise leftover silicon area that was not needed in this work.

The IC was glued to a PCB mounted at 10 mm from the Tx PCB as shown in the picture of Fig. 15. In order to emulate the situation in a monitoring system for power semiconductor modules where the sensors would be mounted some distance above a ground plane, the Rx PCB included a buried ground plane at a depth of 1.6 mm. This plane was also included in all simulations presented in this paper. To reduce the amount of induced current at sensitive nodes, the length of bond wires were kept to a minimum and the circuit goes directly down through vias at the bond wire pads to the bottom layer of the PCB, where the load resistor, R_L , and voltage follower were placed as closely as possible to the vias.

The diode characterisation described in the previous subsection was used to estimate the power transfer efficiency, $\eta = P_L/P_S$ based on observed voltages, V_L , at R_L for different values of load resistance. For each load resistance point, the power was increased until a V_L of 300 mV was obtained. The load resistances used ranged from $560\ \Omega$ to 100 k Ω . Due to the excessive power requirements, it was not possible to drive the PCB coil at lower resistances without overheating it. Therefore the power transfer efficiency characterisation was repeated

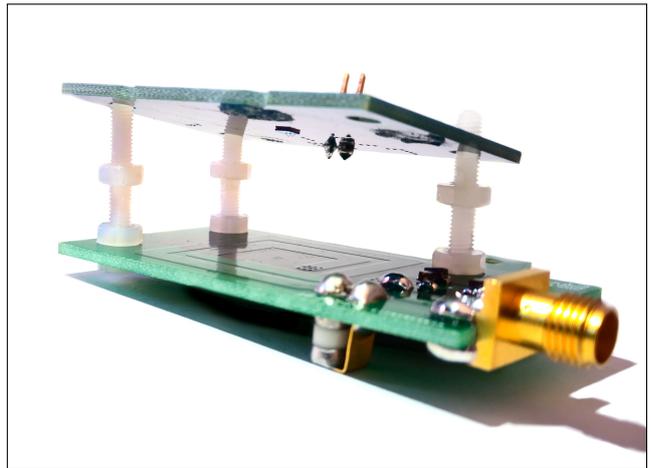


Fig. 15 PCB with IC with on-chip coil on the bottom side mounted 10 mm above PCB with Tx coil.

for a two-turn, wire-wound air coil used as Tx coil and placed directly around the Rx chip as shown in the picture of in Fig. 16. Because of the closer proximity and higher Q factor of the wire coil, a higher efficiency was achieved and it was possible to perform the measurements for load resistances down to $R_L' = 56\ \Omega$. Because of the weak coupling between Tx and Rx coils, as is also the case for the PCB coil variant of this set-up, the resistance at the Rx side is insignificant for the Tx coil. Therefore, the power transfer efficiencies for the two cases (PCB coil and wire coil) should differ by a constant factor over the full resistance range. For the performed measurements, this factor was estimated to approximately 6 dB. Fig. 17 shows a plot of the power transfer efficiency from both types of measurement as a function of load resistance along with circuit simulations based on coil parameters given by electromagnetic simulations. These simulations use the same layer structure and material properties as the simulations presented in Section 4, except that air was used in place of the silicone gel. The power transfer efficiency for the wire coil has been shifted downwards by 6 dB and thus shows the expected behaviour of the PCB coil to be seen had measurements been done for lower load resistances.

Comparing the measurements with simulated values, Fig. 17 shows close agreement in general behaviour of the two graphs. However, the measured values differ by an approximately constant value between 5 and 12 dB. This discrepancy can have several explanations:

One possible explanation could be that because the Tx coil is of very low impedance, the ESR of the matching components may be significant because they are comparable in size to the coil impedance. ESR values of $R_{L,m} = 53\ \text{m}\Omega$ and $R_{C,m} = 35\ \text{m}\Omega$ for the matching shunt inductor, $L_{m,Tx}$, and series capacitor, $C_{m,Tx}$, re-

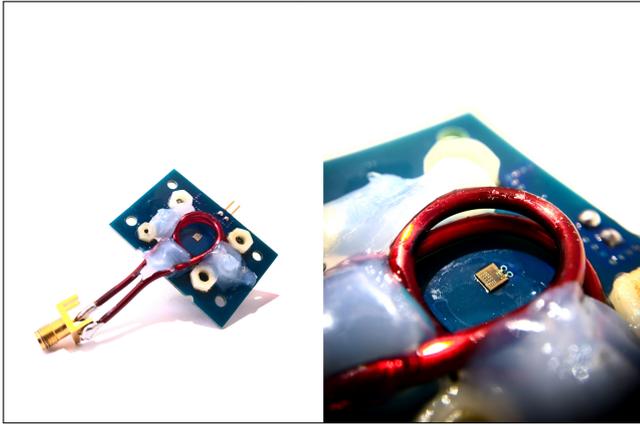


Fig. 16 Wire coil glued around IC with on-chip coil.

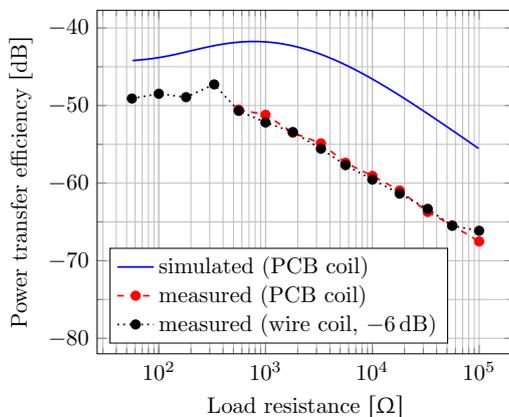


Fig. 17 Simulated and measured values of the power transfer efficiency in an inductive link between two coils for various load resistances. The measurements for the wire coil have been shifted downwards by 6 dB to facilitate comparison with the PCB coil measurements.

spectively, were obtained from data sheets. These are comparable to the ESR of the Tx coil of $R_{Tx} = 573 \text{ m}\Omega$ and are thus likely significant, but circuit simulations show that they are unlikely to be the full explanation for the discrepancy in power transfer efficiency.

Another possibility could be that the DC characterisation of the MOSFET diode is not valid for the high-frequency case. However, no unexpected power consumption in the diode is visible in circuit simulations. It is however possible that the simulator omits effects such as those from the parasitic body diode which would exhibit a significant turn-off time due to the reverse-recovery effect [20] than a pure MOSFET diode and thus result in an increased reverse-leakage current during the negative half-cycles of the transmitted signal. To examine whether this was the case, the coils were immersed in liquid nitrogen in order to cool them down to $-196 \text{ }^\circ\text{C}$. Because the reverse-recovery time in p-n junctions is proportional to absolute temperature [20],

if p-n junction leakage is in fact a problem, it should be heavily mitigated by the lower temperature. However, the power transfer efficiency increased by merely 5 dB for the nitrogen-cooled coils, which is less than what is expected due to decreased resistance in the copper traces of the coils at the reduced temperature, which amounts to approximately 7 dB. Thus, the possibility of parasitic body diode turn-on being the main contributing factor is ruled out. Another characterisation of the MOSFET diode was performed with the diode immersed in liquid nitrogen in order to take into account changes in forward voltage, V_D , of the diode in the calculations.

Another source of error could be that bond wires reaching over the IC coil in order to connect the rectified voltage, V_L , to the load resistor, R_L , could reduce the power transfer efficiency because some energy transmitted by the PCB coil is absorbed by the bond wire loop instead of the IC coil. However, because of the weak coupling between the PCB and IC coils—the latter which is located very near the bond wires whose coupling with the PCB coil should therefore also be weak—this effect should be small. However, it is expected that the coupling between the IC coil and the bond wires is stronger and thus that the bond wires, loaded by, R_L could consume some of the stored magnetic energy in the IC coil, reducing its Q factor, as well as affecting the rectifier's ability to rectify the induced voltage by superimposing a voltage, $v_1(t)$, on V_L . $v_1(t)$ will arrive in phase with the induced voltage, $v_{emf}(t)$, and will thus make it harder for the rectifier to rectify $v_{emf}(t)$. The bond wire loop is estimated to occupy around 2.5% of the IC coil area, resulting in a voltage conversion factor of $0.025k_{Rx-BW}$, where k_{Rx-BW} is the coupling coefficient between the IC coil and the bond wire loop. Although k_{Rx-BW} is expected to be somewhat stronger than the coupling between the two coils, it is still expected to be small. Thus, it is likely that this phenomenon has only a minor effect on the power transfer efficiency.

It is also possible that the accuracy of the electromagnetic model is responsible for the discrepancy. The dielectric materials in the model are modelled as infinite layers in order to speed up the simulations. Had a full 3-dimensional (3D) model been used, it is possible that the accuracy could have been increased.

Furthermore, the manufacturing tolerances for the thicknesses of the layers in the manufactured ICs are large, thus it is possible that parasitic elements such as e.g. substrate capacitance are more prominent than the simulation model shows.

In conclusion, we have identified some possible sources of errors in an attempt to explain the discrepancy between simulation models and measurement results. While it is difficult to say exactly which sources are

most significant it is likely that the discrepancy does not have a single cause, but is rather a combination of multiple sources of error. However, we note again that the graphs exhibit a good matching in overall shape.

6 Conclusion

We have shown theoretically that for the low-power operation of on-chip coils with shunt capacitors as matching networks, there is a limit for where it is inefficient to further decrease the load in an attempt to reduce the transmitted power, and that beyond this limit the optimal coil geometry no longer depends on the load resistance. For the 350 nm CMOS process used in this paper, this limit appears to lie around 56 k Ω . This means that IC sensor systems powered by on-chip coils manufactured in this process technology, requiring a 1 V supply voltage and measuring $2 \times 2 \text{ mm}^2$ would not benefit of decreasing the power budget below about 20 μW . Simulations show that such a power budget can be achieved at a transmitter power, P_S , of 20 dBm. If the discrepancy between simulated and measured results is accounted for, P_S amounts to 32 dBm (1.6 W), which is reasonable for a PCB coil. These values correspond to a power transfer efficiency of -39 dB, as seen in Fig. 8 at $R_L' = 56 \text{ k}\Omega$.

We argue that a power budget in the 20 μW range is reasonable for our application—a temperature monitoring system for power semiconductor modules. As an example, using the temperature sensor presented in [21]—which consumes 14 μW at its highest operating temperature—would leave at least 6 μW for other on-chip systems such as rectifier, analogue-to-digital converter (ADC) and load modulator.

Acknowledgement

The work presented in this paper was funded by Svenska Kraftnät.

Data Availability

The data generated during this study are available from the corresponding author on reasonable request.

References

- Zargham, M., Gulak, P.: Fully integrated on-chip coil in 0.13 μm CMOS for wireless power transfer through biological media. *Biomedical Circuits and Systems, IEEE Transactions on* **9**(2), 259–271 (2015). DOI 10.1109/TBCAS.2014.2328318
- Feng, P., Yeon, P., Cheng, Y., Ghovanloo, M., Constantinou, T.G.: Chip-scale coils for millimeter-sized bioimplants. *IEEE Transactions on Biomedical Circuits and Systems* pp. 1–12 (2018). DOI 10.1109/TBCAS.2018.2853670
- Khalifa, A., Karimi, Y., Wang, Q., Garikapati, S., Montlouis, W., Stanaćević, M., Thakor, N., Etienne-Cummings, R.: The microbead: A highly miniaturized wirelessly powered implantable neural stimulating system. *IEEE Transactions on Biomedical Circuits and Systems* **12**(3), 521–531 (2018). DOI 10.1109/TBCAS.2018.2802443
- Khalifa, A., Liu, Y., Karimi, Y., Wang, Q., Eisape, A., Stanaćević, M., Thakor, N., Bao, Z., Etienne-Cummings, R.: The microbead: A 0.009 mm³ implantable wireless neural stimulator. *IEEE Transactions on Biomedical Circuits and Systems* **13**(5), 971–985 (2019). DOI 10.1109/TBCAS.2019.2939014
- Nilsson, J., Borg, J., Johansson, J.: Single chip wireless condition monitoring of power semiconductor modules. In: *Nordic Circuits and Systems Conference (NORCAS): NORCHIP International Symposium on System-on-Chip (SoC)*, 2015, pp. 1–4 (2015). DOI 10.1109/NORCHIP.2015.7364407
- Nilsson, J., Borg, J., Johansson, J.: Chip-coil design for wireless power transfer in power semiconductor modules. In: *2018 2nd Conference on PhD Research in Microelectronics and Electronics Latin America (PRIME-LA)*, pp. 1–4 (2018). DOI 10.1109/PRIME-LA.2018.8370384
- Chen, K., Zhao, Z.: Analysis of the double-layer printed spiral coil for wireless power transfer. *IEEE Journal of Emerging and Selected Topics in Power Electronics* **1**(2), 114–121 (2013). DOI 10.1109/JESTPE.2013.2272696
- Ji, B., Pickert, V., Cao, W., Xing, L.: Onboard condition monitoring of solder fatigue in IGBT power modules. In: *Diagnostics for Electric Machines, Power Electronics and Drives (SDEMPED)*, 2013 9th IEEE International Symposium on, pp. 9–15 (2013). DOI 10.1109/DEMPE.2013.6645690
- Held, M., Jacob, P., Nicoletti, G., Scacco, P., Poech, M.H.: Fast power cycling test of IGBT modules in traction application. In: *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1, pp. 425–430 vol.1 (1997). DOI 10.1109/PEDS.1997.618742
- Yang, S., Xiang, D., Bryant, A., Mawby, P., Ran, L., Tavner, P.: Condition monitoring for device reliability in power electronic converters: A review. *Power Electronics, IEEE Transactions on* **25**(11), 2734–2752 (2010). DOI 10.1109/TPEL.2010.2049377
- Oh, H., Han, B., McCluskey, P., Han, C., Youn, B.: Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review. *Power Electronics, IEEE Transactions on* **30**(5), 2413–2426 (2015). DOI 10.1109/TPEL.2014.2346485
- Wolfgang, E.: Examples for failures in power electronics systems. *ECPE tutorial on reliability of power electronic systems*, Nuremberg, Germany (2007)
- Hoer, C., Love, Y.: Exact inductance equations for rectangular conductors with applications to more complicated geometries. *J. Res. Nat. Bureau Standards-C. Eng. Instrum.* **69**(2), 127–137 (1965)
- Say, M.G.: *Alternating Current Machines*, fourth edn. Pitman Publishing Limited (1976)
- Wheeler, H.A.: Simple inductance formulas for radio coils. *Proceedings of the Institute of Radio Engineers* **16**(10), 1398–1400 (1928). DOI 10.1109/JRPROC.1928.221309
- Kuhn, W.B., Yanduru, N.K.: Spiral inductor substrate loss modeling in silicon RF ICs. In: *Proceedings RAW-*

- CON 98. 1998 IEEE Radio and Wireless Conference (Cat. No.98EX194), pp. 305–308 (1998). DOI 10.1109/RAWCON.1998.709197
17. Nilsson, J., Borg, J., Johansson, J.: Maximal Q factor for an on-chip, fuse-based trimmable capacitor. *Electronics* **8**(1), 62 (2019). DOI 10.3390/electronics8010062. URL <http://dx.doi.org/10.3390/electronics8010062>
 18. FEKO: version 7.10.0 (R2010a). EM Software and Systems-S.A. (Pty) Ltd (2015)
 19. Swedish Post and Telecommunications Authority: Post- och telestyrelsens allmänna råd (ptsfs 2015:3) om den svenska frekvensplanen (2015). URL https://pts.se/globalassets/startpage/dokument/legala-dokument/foreskrifter/radio/ptsfs-2015_3-allmanna-rad-frekvensplanen.pdf
 20. Fink, H.: Reverse recovery time measurements of epitaxial silicon p-n junctions at low temperatures. *Solid-State Electronics* **7**(11), 823 – 831 (1964). DOI [https://doi.org/10.1016/0038-1101\(64\)90134-0](https://doi.org/10.1016/0038-1101(64)90134-0)
 21. Nilsson, J., Borg, J., Johansson, J.: High-temperature characterisation and analysis of leakage-current-compensated, low-power bandgap temperature sensors. *Analog Integrated Circuits and Signal Processing* (2017). DOI 10.1007/s10470-017-1011-6. URL <https://doi.org/10.1007/s10470-017-1011-6>