Leakage Current Compensation for a 450 nW, High-Temperature, Bandgap Temperature Sensor

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***Abstract*—The design of a 450 nW bandgap temperature sensor in the 0 to 175 °C range is presented. The design demonstrates a leakage current compensation technique that is useful for low-power designs where transistor performance is limited. The technique mitigates the effects of leakage in Brokaw bandgap references by limiting the amount of excess current that is entering the bases of the main bipolar pair due to leakage. Using this technique, Monte Carlo simulations show an improvement factor of 7.6 for the variation of the temperature sensitivity over the full temperature range. For the variation of the reference voltage, Monte Carlo simulations show an improvement factor of 2.3.**

Sensors built using this technique can be used to accurately monitor the temperature of power semiconductors since wireless temperature sensors become feasible with sufficiently low power consumption.

***Index Terms*—bandgap, temperature sensor, voltage reference, low power, high temperature, leakage current**

I. Introduction

In this work, the design of a low-power, high-temperature CMOS temperature sensor is presented. The target is to monitor the temperature of power semiconductors in order to predict failures of power electronic equipment. Many emerging power semiconductor faults, especially those related to the packaging of a device, manifest themselves as a temperature rise [1]. Thus, monitoring of temperature of a device can enable early fault detection and preventive maintenance. An example of a package fault is solder fatigue, where the solder that attaches the power semiconductor to its cooling base plate degenerates, resulting in reduced cooling efficiency [2].

Monitoring of high power devices can be challenging as the operating range is often specified to high temperatures. Such high temperatures introduce non-linearities in standard temperature sensors due to leakage currents in hot parasitic reverse-biased p-n junctions. These currents increase exponentially with temperature, making them particularly difficult to deal with in high-temperature applications. Methods exist to compensate for the effects of leakage currents [3]–[5], but additional compensation may be required when low-power sensors are operated at high temperatures.

Due to challenges with galvanic isolation, high voltages in power semiconductors complicate the process of measuring die temperature. For this reason, indirect measurement methods have been developed [1]. Three such methods were demonstrated in [6], where different parameters were measured and used to estimate the junction temperature of a power MOSFET device. Drawbacks of these indirect approaches are that much must be known about the device to measure on and that the obtained measurements may not be as accurate as direct measurements would be.

Using wireless technology, challenges with galvanic isolation can be avoided. The limited amount of power available in a wireless sensor places stringent demand on its power consumption. Low-power operation at high temperatures is particularly challenging since leakage currents increase exponentially with temperature and become a serious problem when their magnitude approaches that of the circuit's quiescent current.

This paper presents the design and simulations of a $450\,\mathrm{nW}$ CMOS chip for the generation of a proportional to absolute temperature (PTAT) voltage as well as a stable bandgap reference voltage in the 0 to $175\,^{\circ}\mathrm{C}$ range. The circuit incorporates a leakage current compensation technique, where a Brokaw bandgap reference [7] is used as a base, and focus is put on combining high-temperature measurements with low-power operation. In particular, the effects of leakage current are studied and leakage current compensation techniques are discussed and simulated. The results will be used as a base in the design of a wireless temperature measurement system for power semiconductors.

In Section II, this paper presents an overview of the operation of the Brokaw bandgap reference. Emphasis is put on how leakage currents affect circuit operation and how previous work has compensated for leakage currents. In Section III, a circuit is presented to demonstrate a leakage current compensation technique. In Section IV, simulation results of said circuit are presented with discussions in Section V. Conclusions are presented in Section VI.

II. The Brokaw Bandgap Reference

The Brokaw bandgap reference [7], an implementation of which is depicted in Fig. 1, is a commonly used circuit for accurately measuring temperature or for providing a temperature insensitive bandgap voltage. It operates by having MOS transistors M_3, M_4, and M_5 enforce equal collector currents, I_{C1} and I_{C2}, through the bipolar pair, Q_1 and Q_2, while relying on differently sized emitter areas to produce a PTAT voltage, V_{PTAT}, over resistance R_2 and a temperature-independent reference voltage, V_{REF}, at the bases of the bipolar pair. V_{REF} is the result of the summation of V_{PTAT} and the

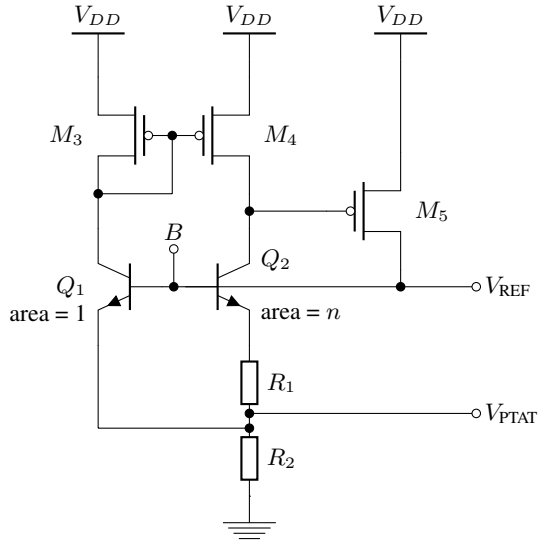

Fig. 1. Brokaw bandgap reference circuit. For simplicity, the start-up circuit has been omitted.

complementary to absolute temperature (CTAT) base-emitter (BE) voltage of Q_1, V_{BE1}. In order for V_{REF} to be temperature insensitive, $\partial V_{\text{PTAT}}/\partial T$, which is positive, must be controlled so that it cancels out $\partial V_{BE1}/\partial T$, which is negative. This can be done by adjusting the ratio between the resistances R_1 and R_2.

A. Leakage Currents in Brokaw Bandgap References

Leakage currents in reverse-biased p-n junctions increase exponentially with temperature. This introduces challenges for circuit designers who design for the high temperature range. A particular challenge with the Brokaw bandgap reference is that the collector-substrate (CS) leakage currents of Q_1 and Q_2 differ in magnitude due to differing transistor sizes. This size mismatch results in a mismatch in collector currents. Since an essential part in proper circuit operation is the assumption of equal collector currents, leakage currents will cause V_{PTAT} to become less linear at high temperatures. This non-linearity will also be present in V_{REF}, since V_{REF} is the sum of V_{PTAT} and V_{BE1}.

B. Earlier Work in Leakage Current Compensation Techniques

To mitigate the effects of leakage currents in bandgap circuits, Radoiaş et al. introduced a leakage current compensation technique in 2012 and used it to produce a Widlar bandgap circuit [8] with improved temperature dependence [4]. In 2013, the same group used said technique to improve the temperature dependence of a Brokaw bandgap circuit [5].

The latter circuit introduced an additional transistor having a shorted BE junction connected to the emitter of Q_1 and its collector to the collector of Q_1. In this way, the new transistor is operated in cut-off mode and therefore does not affect circuit operation, but is still under the effect of the same CS leakage current phenomenon as are Q_1 and Q_2. If the emitter area of the new transistor equals the difference between the emitter areas of Q_1 and Q_2, then the leakage current from the collector nodes roughly match, and the only remaining mismatches are those which result from mismatches in device parameters and reverse-voltages. This technique has the effect that it reduces the magnitude of the non-linearities resulting from mismatches in collector currents.

C. Leakage-Induced Excess Base Current

In the works referenced in Section II-B, Radoiaş et al. do not mention any effect that the leakage of the reverse-biased collector-base (CB) junctions of Q_1 and Q_2 or the reverse-biased body-drain (BD) junction of M_5 have on circuit operation, nor do they compensate for such leakage. A non-linearity, which is the main topic of this work, can result from the leakage currents produced from said junctions. These leakages cause excess current to be introduced at the bases of the bipolar pair, node B. Leakage introduced at node B has a particularly severe effect on circuit operation since any excess current introduced there is amplified by the bipolar transistors.

Assume that the collector current of Q_1, I_{C1}, changes due to CB or BD leakage and current amplification in Q_1. This change in current will change the voltage at the collector of Q_2 due to the current mirror action of M_3 and M_4. That voltage signal will in turn be amplified by the common-source amplifier, M_5. The majority of the change in output current from M_5 will take the path through the BE junction of Q_1 since that path has lower impedance than the path through the BE junction of Q_2, since Q_1 is biased at a higher current density and has no series resistor. This current will be amplified by Q_1 and counteract the initially assumed change of I_{C1}. Neglecting the Early effect of Q_2, the loop gain along the feedback path, A_L, is proportional to $r_{o4}g_{m5}\beta_1$, where r_{o4} is the small signal output resistance of M_4, g_{m5} is the small signal transconductance of M_5, and β_1 is the current gain of Q_1. It is a challenge to achieve high loop gain for low power designs since all variables in the expression for A_L benefit from higher power levels.

If A_L is not high enough, a change in I_{C1} is not reduced to a negligible amount and the currents I_{C1} and I_{C2} will not be equal. Therefore, the assumption made in the beginning of this section about equal collector currents no longer holds, resulting in non-linearities being introduced in the output voltages V_{REF} and V_{PTAT}.

III. Circuit Design

To compensate for excess current leaking into node B in Fig. 1, a source of artificial leakage current can be introduced, leaking out the same amount of current from the node that is leaking into it. This can be achieved with a current mirror and cut-off transistors with dimensions equal to those of Q_1, Q_2 and M_5. The purpose of the cut-off transistors is to replicate the leakage current of the ordinary transistors.

A. Proposed Circuit

In 1998, Mizuno et al. [3] proposed a technique to create a source of artificial leakage current. This technique takes into

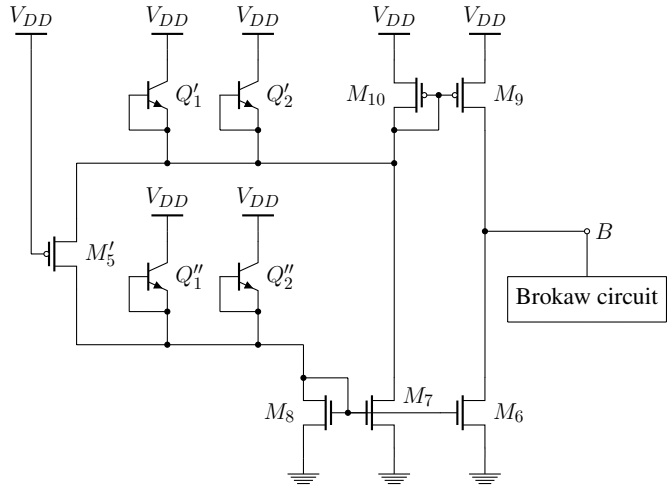

Fig. 2. Compensation circuit connected to the Brokaw bandgap circuit from Fig. 1. The prim/bis notation denotes devices identical to similarly named devices from the Brokaw bandgap circuit depicted in Fig. 1. Figure corrected after publication.

account differences in reverse-voltages between p-n junctions in replicas and ordinary transistors, resulting in better matching between original and artificial leakage currents compared to only using a current mirror. In this work, we apply the technique of Mizuno et al. to minimise the net excess current entering node B due to leakage. Specifically, replicas of transistors Q_1, Q_2 and M_5 are added and used as input to a PMOS version of the precise circuit from [3], the output of which is connected to node B. The resulting circuit is depicted in Fig. 2. The bipolar replicas, Q_1', Q_2', Q_1'' and Q_2'' are made to operate in cut-off mode by connecting their collectors to V_{DD} while shorting their BE junctions and connecting them to the compensation circuit. The MOSFET replica, M_5', is made to operate in cut-off mode by connecting its gate to V_{DD} while connecting its drain and source to the compensation circuit. Two sets of replicas are needed for the bipolar transistors since the compensation circuit operates by measuring the leakage current produced by two p-n junctions. This is not the case for the MOSFET replica, as both its source and drain can be used as input to the compensation circuit.

B. Transistor Dimensions

For a $0.18\,\mu\mathrm{m}$ design, transistor dimensions from the circuits of Fig. 1 and Fig. 2 are summarised in Table I.

In order to minimise leakage current, transistor widths for MOSFETs should be small since that results in smaller areas of reverse-biased BD junctions. On the other hand, small width increases the overdrive voltage for a given drain current, which increases the required supply voltage and therefore the power consumption. As a compromise between these two constraints, all MOSFETs have a width of $2\,\mu\mathrm{m}$.

A short length of the mirroring transistors M_3 and M_4 reduces the output resistance of the current mirror, lowering the loop gain, A_L. A long length would increase the overdrive voltage of said transistors, increasing required supply voltage.

TABLE I
DIMENSIONS OF TRANSISTORS FROM THE CIRCUITS OF FIG. 1 AND FIG. 2 FOR A $0.18\,\mu\mathrm{m}$ DESIGN.

Device		
MOSFETs	*width* [nm]	*length* [nm]
M_3, M_4	2000	360
M_5	2000	720
M_6, M_7, M_8, M_9, M_{10}	2000	3600
BJTs	*emitter area* [$\mu\mathrm{m}^2$]	
Q_1	6.8	
Q_2	40.8	

As a compromise between these two constraints, M_3 and M_4 have a length of $360\,\mathrm{nm}$.

Matching collector voltages of Q_1 and Q_2 allows for better matching of leakage currents for the compensation technique of Radoiaş et al. [5] due to matching reverse voltages over CS junctions. Good matching of collector voltages can be achieved if the length of M_5 is increased compared to M_3 and M_4. M_5 has a smaller drain current and therefore requires longer length for the same gate voltage. Because of smaller drain current, the overdrive voltage of M_5 does not increase the required supply voltage for sufficiently short length such as $720\,\mathrm{nm}$ as used in this design.

For transistors M_6, M_7, M_8, M_9, and M_{10} in the compensation circuit of Fig. 2, a higher overdrive voltage than for M_3, M_4, and M_5 can be afforded since the full supply voltage is available to them. A longer length results in higher output resistance and therefore better leakage current matching. Those transistors have a length of $3.6\,\mu\mathrm{m}$.

The emitter area of Q_1 is of the minimum size available in the process library, $6.8\,\mu\mathrm{m}^2$. In accordance with common practice in bandgap circuit design, the emitter area of Q_2 is 6 times that size, $40.8\,\mu\mathrm{m}^2$.

IV. Simulation Results

A chip design was created in a $0.18\,\mu\mathrm{m}$ process, based on the circuit described in Section III. All bipolar devices were implemented using vertical bipolar junction transistors. Parasitics were extracted from the design and simulations of the resulting circuit were run.

For both the compensated and uncompensated circuits from Fig. 2 and Fig. 1, respectively, Fig. 3 shows a plot of the reference voltage, V_{REF}, as a function of temperature. It can be seen that the uncompensated voltage increases exponentially for high temperatures, whereas the compensated voltage is affected only marginally even in the high-temperature range. Over the full temperature range, V_{REF} varies $17.1\,\mathrm{mV}$ for the uncompensated circuit, compared to $1.9\,\mathrm{mV}$ for the compensated circuit.

In Fig. 4, a similar plot is shown for the temperature sensitivity of the PTAT voltage, $\partial V_{\mathrm{PTAT}}/\partial T$. For the high-temperature range, an observation similar to the one made for V_{REF} can be made for $\partial V_{\mathrm{PTAT}}/\partial T$, but in this plot,

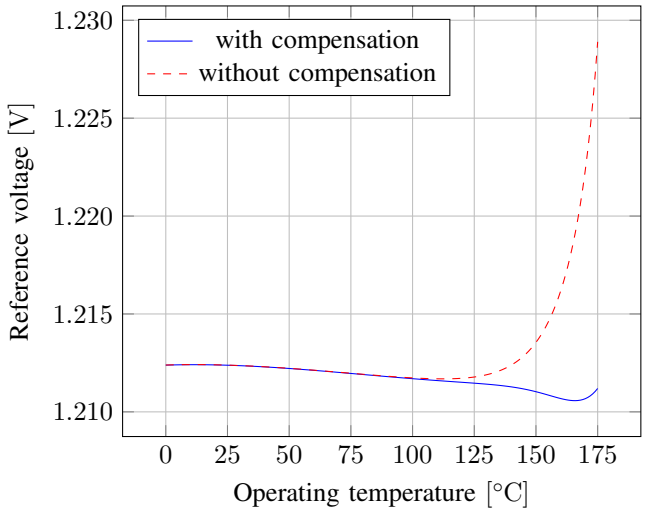

Fig. 3. Simulation result of the reference voltage, V_{REF}, as a function of operating temperature for a Brokaw bandgap reference (Fig. 1) with and without compensation circuit (Fig. 2).

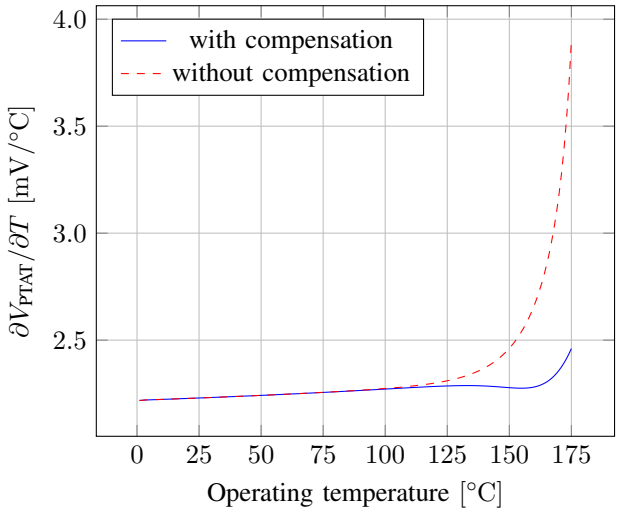

Fig. 4. Simulation result of the temperature sensitivity of the PTAT voltage, $\partial V_{\text{PTAT}}/\partial T$, as a function of operating temperature for a Brokaw bandgap reference (Fig. 1) with and without compensation circuit (Fig. 2).

the non-linearity for the compensated circuit is more clearly visible. Over the full temperature range, $\partial V_{\text{PTAT}}/\partial T$ varies $1.66\,\text{mV}/°\text{C}$ for the uncompensated circuit, compared to $243\,\mu\text{V}/°\text{C}$ for the compensated circuit.

For the compensated circuit, a plot of the power consumption as a function of operating temperature is shown in Fig. 5. It can be seen that for low temperatures the power consumption is a linear function of temperature, while for high temperatures a superimposed exponential component is seen.

Main performance parameters for both compensated and uncompensated circuits extracted from Monte Carlo simulations are summarised in Table II. From the table, it can be seen that adding the compensation circuit does not adversely affect the accuracy of the reference voltage or the temperature sensitivity.

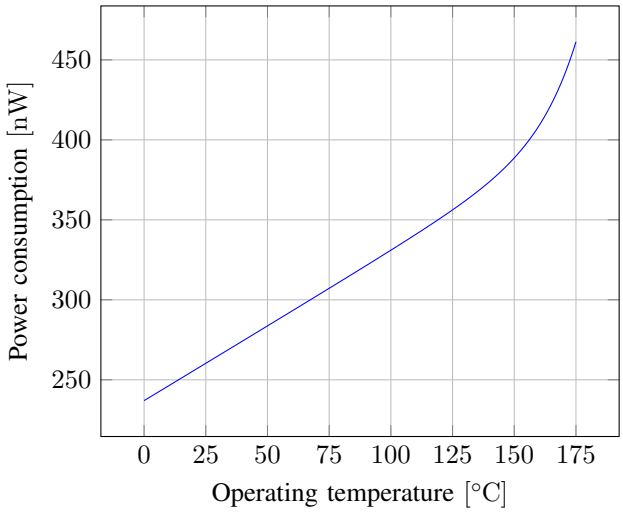

Fig. 5. Simulation result of the power consumption as a function of operating temperature for a Brokaw bandgap reference (Fig. 1) with compensation circuit (Fig. 2). The circuit was operated with a power supply of 2 V.

TABLE II
SUMMARY OF PARAMETERS OBTAINED FROM A 100-SAMPLE MONTE CARLO SIMULATION OF BOTH COMPENSATED AND UNCOMPENSATED CIRCUITS. 'AVERAGE VALUE' IS THE AVERAGE TAKEN OVER THE FULL TEMPERATURE RANGE. 'MAX/MIN VARIATION' IS THE DIFFERENCE BETWEEN THE MAXIMUM AND MINIMUM VALUES IN THE FULL TEMPERATURE RANGE. VALUES FOR THE POWER CONSUMPTION ARE GIVEN FOR A POWER SUPPLY OF 2 V.

Parameter	**Uncompensated**		**Compensated**	
Reference voltage	*mean*	*std. dev.*	*mean*	*std. dev.*
Average value [V]	1.227	0.1054	1.213	0.0987
Max/min variation [mV]	21.95	6.892	9.430	6.847
$\partial V_{\text{PTAT}}/\partial T$	*mean*	*std. dev.*	*mean*	*std. dev.*
Average value [mV/°C]	2.360	0.061 30	2.254	0.058 43
Max/min variation [µV/°C]	1950	808.2	258.2	67.39
Power consumption [nW]	*mean*	*std. dev.*	*mean*	*std. dev.*
at 27 °C	264.8	30.94	262.4	32.64
at 175 °C	441.1	35.07	438.9	36.40

V. DISCUSSION

In this section, various aspects of the proposed circuit are analysed and compared with other work.

A. Compensation Circuit Power Consumption

The compensation circuit consumes current of the same order of magnitude as the current it is compensating for. Therefore, a small increase in power consumption could be expected for high temperatures. If there is such an increase, it is too small to be significant for the Monte Carlo simulations performed in this work, as no significant difference in power consumption can be seen in Table II between the compensated and uncompensated cases.

B. Total Power Consumption Characterisation

As can be seen in Fig. 5, for low temperatures, the total power consumption, P_{TOT}, is a linear function of temperature, but increases more rapidly for higher temperatures. This behaviour can be explained by realising that P_{TOT} consists of two main parts, P_Q and P_{LEAK}. P_Q is the power consumed due to the quiescent current, I_Q, used to bias transistors Q_1 and Q_2, while P_{LEAK} is the power consumed by leakage currents and the compensation.

The quiescent current, I_Q, is determined by resistor R_2. Since the voltage over R_2, V_{PTAT}, is proportional to absolute temperature, the current through it, $I_2 = I_Q$, is also proportional to absolute temperature, $I_Q \propto T$. I_Q is supplied by V_{DD}, so the power consumption resulting from it, P_Q, equals $I_Q \cdot V_{DD}$. Therefore, assuming V_{DD} is constant, $P_Q \propto T$.

The total amount of leakage current, I_{LEAK}, is exponentially related to temperature. Under the assumption that leaked current does not change the voltages over which it is leaking, P_{LEAK} will be proportional to I_{LEAK}, hence $P_{\text{LEAK}} \propto e^T$.

Since the magnitude of the leakage current is small for low temperatures, P_Q will dominate the power consumption in the low temperature range while, for high temperatures, P_{LEAK} can contribute significantly. Therefore, attempting to reduce I_Q below a certain value in order to decrease power consumption will be ineffective for the high-temperature range.

C. Comparison with Other Work

At higher power levels other works have demonstrated results similar to the results of this work. An example is [4], where the same temperature range as in this work was achieved, but with at least 10 times the power consumption.

Sensors that achieve higher operating temperatures do so with further increased power consumption. For example, [9] is characterised up to $225\,^{\circ}\text{C}$ at a power consumption of $112.5\,\mu\text{W}$, while [10] is characterised up to $200\,^{\circ}\text{C}$ at a power consumption of $40\,\mu\text{W}$. Both of these sensors were fabricated in silicon on insulator (SOI) processes, for which high-temperature design is facilitated due to lower leakage currents. SOI-technology could be used to further extend the temperature range of the sensor presented in this work.

The authors are not aware of bandgap circuits that achieve lower power consumption than the sensor presented in this work, neither are they aware of sensors using other topologies that achieve lower power consumption and are characterised in the same high-temperature range as the sensor from this work. Two examples that achieve lower power consumption include [11] and [12], which are only characterised up to $100\,^{\circ}\text{C}$ and $60\,^{\circ}\text{C}$, respectively.

VI. Conclusion

A leakage current compensation circuit [3] is used in a Brokaw bandgap circuit in order to minimise the net amount of excess current leaking into the bases of its main bipolar transistors. This results in improved linearity with respect to temperature for the reference voltage and the PTAT voltage. The technique is useful for circuits whose devices have low gain, e.g. low-power circuits, and can be used to extend the operating temperature range of bandgap temperature sensors or bandgap references.

For the bandgap circuit depicted in Fig. 1, simulation results over the 0 to $175\,^{\circ}\text{C}$ temperature range show that the variation of the reference voltage was improved from $17.1\,\text{mV}$ to $1.9\,\text{mV}$, while the variation of the temperature sensitivity was improved from $1.66\,\text{mV}/^{\circ}\text{C}$ to $243\,\mu\text{V}/^{\circ}\text{C}$ when the compensation circuit from Fig. 2 was added.

The technique will be used to enable accurate condition monitoring of power semiconductor devices through wireless power and data transfer.

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